

L-A780 Ver:0.3 (MS-7389L2 Ver:0C)

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CPU:

AMD AM2+
AMD AMD Athlon 64 X2
AMD Athlon 64 FX
AMD Athlon 64
AMD Sempron CPUs



System Chipset:

AMD - RS780 (North Bridge)
AMD - SB700 (South Bridge)



On Board Chipset:

BIOS - SPI
Azalia CODEC - Realtek ALC662(Default)/888
LPC Super I/O -- ITE IT8718F(GX)
LAN - Marvell 8039/8056/8071/8075/8070(Default)
IEEE1394 - VIA VT6308P
TMP - WPCT200(Default)/ST19WP18
Asset ID - PCA24S08
HWM W83201G



Main Memory:

DDR II * 4 (Max 4GB)

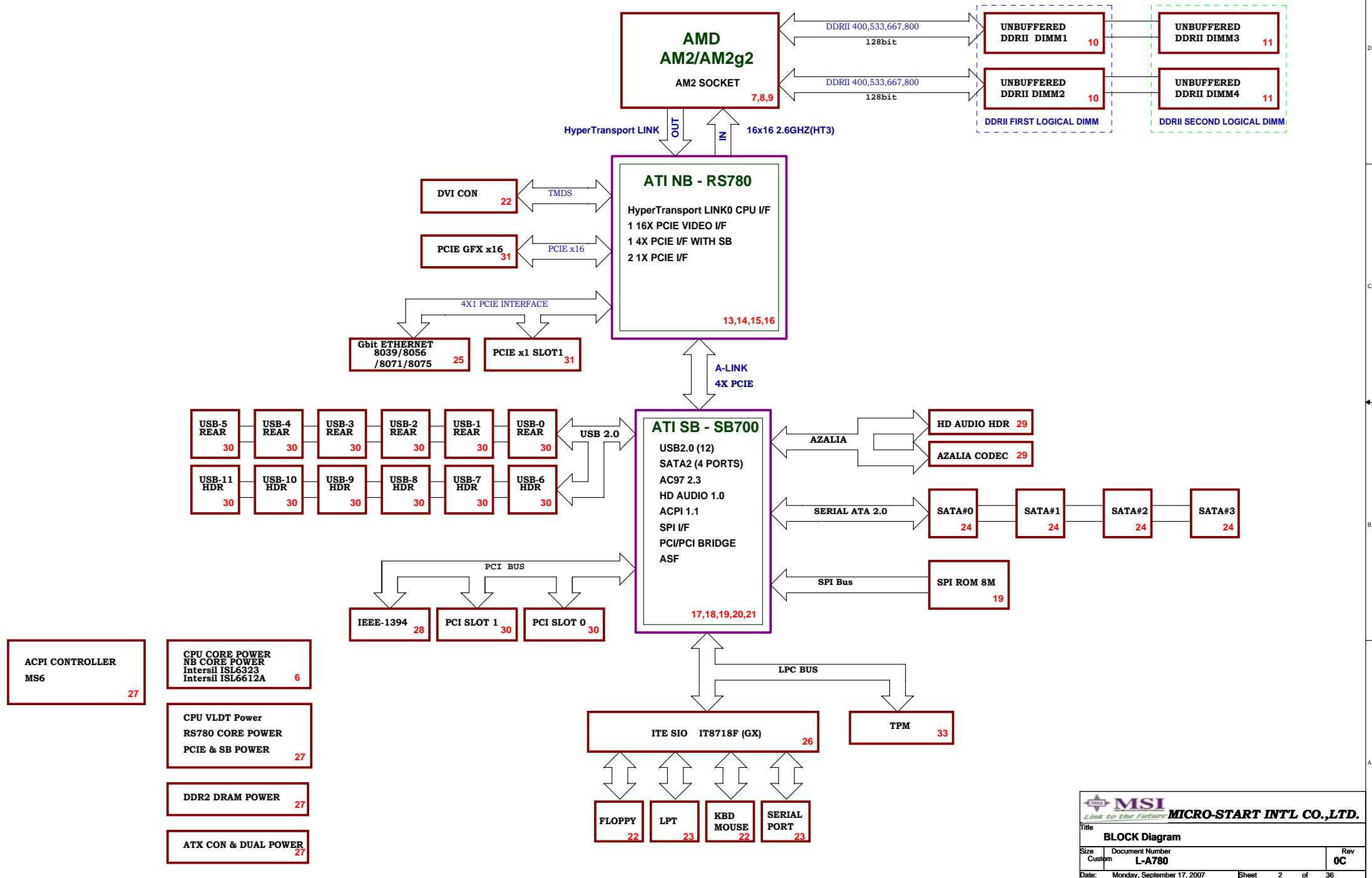
Expansion Slots:

PCI Express X16 Slot * 1
PCI Express X1 Slot * 1
PCI 2.3 Slot * 2

Intersil PWM:

Controller - Intersil 6323 3 Phase

Project RS-780 BLOCK DIAGRAM



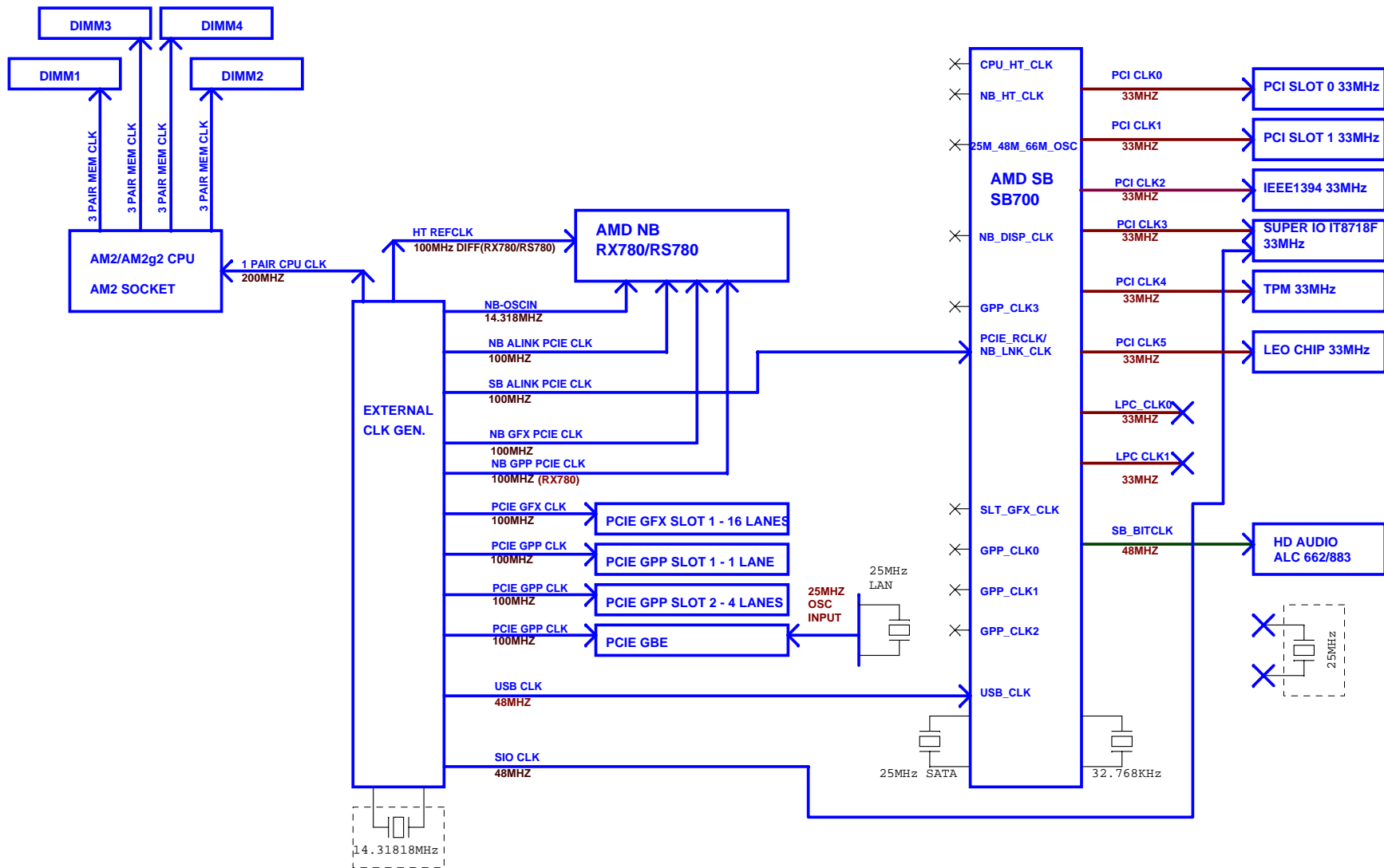
GPIO Name	Type	Function Description	Pin	Page
PCICLK5/GPIO41	3.3V	PCI_CLK5	T3	17
REQ3#/GPIO70		PREQ#3	AE6	17
REQ4#/GPIO71		PREQ#4	AB6	17
GNT3#/GPIO72		Unused	AC6	17
GNT4#/GPIO73		Unused	AE5	17
INTE#/GPIO33		PCI_INTA#	AD3	17
INTF#/GPIO33		PCI_INTB#	AC4	17
INTG#/GPIO33		PCI_INTC#	AE2	17
INTH#/GPIO33		PCI_INTD#	AE3	17
LDRQ1#/GNT5#/GPIO68		Unused	AB8	17
BMREQ#/REQ5#/GPIO65		PREQ#5	AD7	17
R1#/EXTENVTO#		R1#	E2	18
SLP_S2/GPM9#		Unused	H7	18
GA20IN/GEVENT0#		A20GATE	Y15	18
KBRST#/GEVENT1#		KBRST#	W15	18
LPC_PME#/GEVENT3#		LPC_PME#	K4	18
LPC_SMI#/EXTENVT1#		LPC_SMI#	K24	18
S3_STATE/GEVENT5#		Unused	F1	18
SYS_RESET#/GPM7#		FP_RST#	J2	18
WAKE#/GEVENT8#		WAKE#	H6	18
BLINK/GPM6#		Unused	F2	18
SMBALERT#/THRMTrip#/GEVENT2#		SMBALERT#	J6	18
SATA_ISO#/GPIO10		SB_GPIO10(Strapping)	AE18	18
CLK_REQ3#/SATA_IS1#/GPIO6		SB_GPIO6(Strapping)	AD18	18
SMARTVOLT/SATA_IS2#/GPIO4		SB_GPIO4(Strapping)	AA19	18
CLK_REQ0#/SATA_IS3#/GPIO0		SB_GPIO0(Strapping)	W17	18
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39		SB_GPIO39(Strapping)	V17	18
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40		SB_GPIO40(Strapping)	W20	18
SPKR/GPIO2		SPKR	W21	18
SCL0/GPOC0#		SCLK	AA18	18
SDA0/GPOC1#		SDATA	W18	18
SCL1/GPOC2#		SCLK1	K1	18
SDA1/GPOC3#		SDATA1	K2	18
DDC1_SCL/GPIO9		Unused	AA20	18
DDC1_SDA/GPIO8		SPI_WP#	Y18	18
LLB#/GPIO66		LC_SENSE	C1	18
SHUTDOWN#/GPIO5		SB_GPIO5(Strapping)	Y19	18
DDR3_RST#/GEVENT7#		Unused	G5	18
USB_OC6#/IR_TX1/GEVENT6#		OC4#	B9	18
USB_OC5#/IR_TX0/GPM5#		OC4#	B8	18
USB_OC4#/IR_RX0/GPM4#		OC3#	A8	18
USB_OC3#/IR_RX1/GPM3#		OC3#	A9	18
USB_OC2#/GPM2#		OC2#	E5	18
USB_OC1#/GPM1#		OC2#	F8	18
USB_OC0#/GPM0#		OC1#	E4	18
AZ_SDIN0/GPIO42		SDATA_IN_R	J7	18
AZ_SDIN1/GPIO43		Unused	J8	18
AZ_SDIN2/GPIO44		Unused	L8	18
AZ_SDIN3/GPIO46		Unused	M3	18

GPIO Name	Type	Function Description	Pin	Page
AZ_DOCK_RST#/GPM8#		Unused	L5	18
PS2_DAT/EC_GPIO0		Unused	H19	18
PS2_CLK/EC_GPIO1		Unused	H20	18
SPI_CS2#/EC_GPIO2		Unused	H21	18
IDE_RST#/F_RST#/EC_GPO3		Unused	F25	18
PS2KB_DAT/EC_GPIO4		Unused	D22	18
PS2KB_CLK/EC_GPIO5		Unused	E24	18
PS2M_DAT/EC_GPIO6		Unused	E25	18
PS2M_CLK/EC_GPIO7		Unused	D23	18
USBCLK/14M_25M_48M_OSC		USB_48M_CLK	C8	18
KSO_16/EC_GPIO8		Unused	A18	18
KSO_17/EC_GPIO9		Unused	B18	18
EC_PWM0/EC_GPIO10		Unused	F21	18
SCL2/EC_GPIO11		Unused	D21	18
SDA2/EC_GPIO12		Unused	F19	18
SCL3_LV/EC_GPIO13		Unused	E20	18
SDA3_LV/EC_GPIO14		Unused	E21	18
EC_PWM1/EC_GPIO15		Unused	E19	18
EC_PWM2/EC_GPIO16		SB_GP16(Strapping)	D19	18
EC_PWM3/EC_GPIO17		Unused	E18	18
KSI_0/EC_GPIO18		Unused	G20	18
KSI_1/EC_GPIO19		Unused	G21	18
KSI_2/EC_GPIO20		Unused	D25	18
KSI_3/EC_GPIO21		Unused	D24	18
KSI_4/EC_GPIO22		Unused	C25	18
KSI_5/EC_GPIO23		Unused	C24	18
KSI_6/EC_GPIO24		Unused	B25	18
KSI_7/EC_GPIO25		Unused	C23	18
KSO_0/EC_GPIO26		Unused	B24	18
KSO_1/EC_GPIO27		Unused	B23	18
KSO_2/EC_GPIO28		Unused	A23	18
KSO_3/EC_GPIO29		Unused	C22	18
KSO_4/EC_GPIO30		Unused	A22	18
KSO_5/EC_GPIO31		Unused	B22	18
KSO_6/EC_GPIO32		Unused	B21	18
KSO_7/EC_GPIO33		Unused	A21	18
KSO_8/EC_GPIO34		Unused	D20	18
KSO_9/EC_GPIO35		Unused	C20	18
KSO_10/EC_GPIO36		Unused	A20	18
KSO_11/EC_GPIO37		Unused	B20	18
KSO_12/EC_GPIO38		Unused	B19	18
KSO_13/EC_GPIO39		Unused	A19	18
KSO_14/EC_GPIO40		Unused	D18	18
KSO_15/EC_GPIO41		Unused	C18	18
SATA_ACT#/GPIO67		SATA_LED#	W11	19
IDE_D0/GPIO15		Unused	AD24	19
IDE_D1/GPIO16		Unused	AD23	19
IDE_D2/GPIO17		Unused	AE22	19
IDE_D3/GPIO18		Unused	AC22	19

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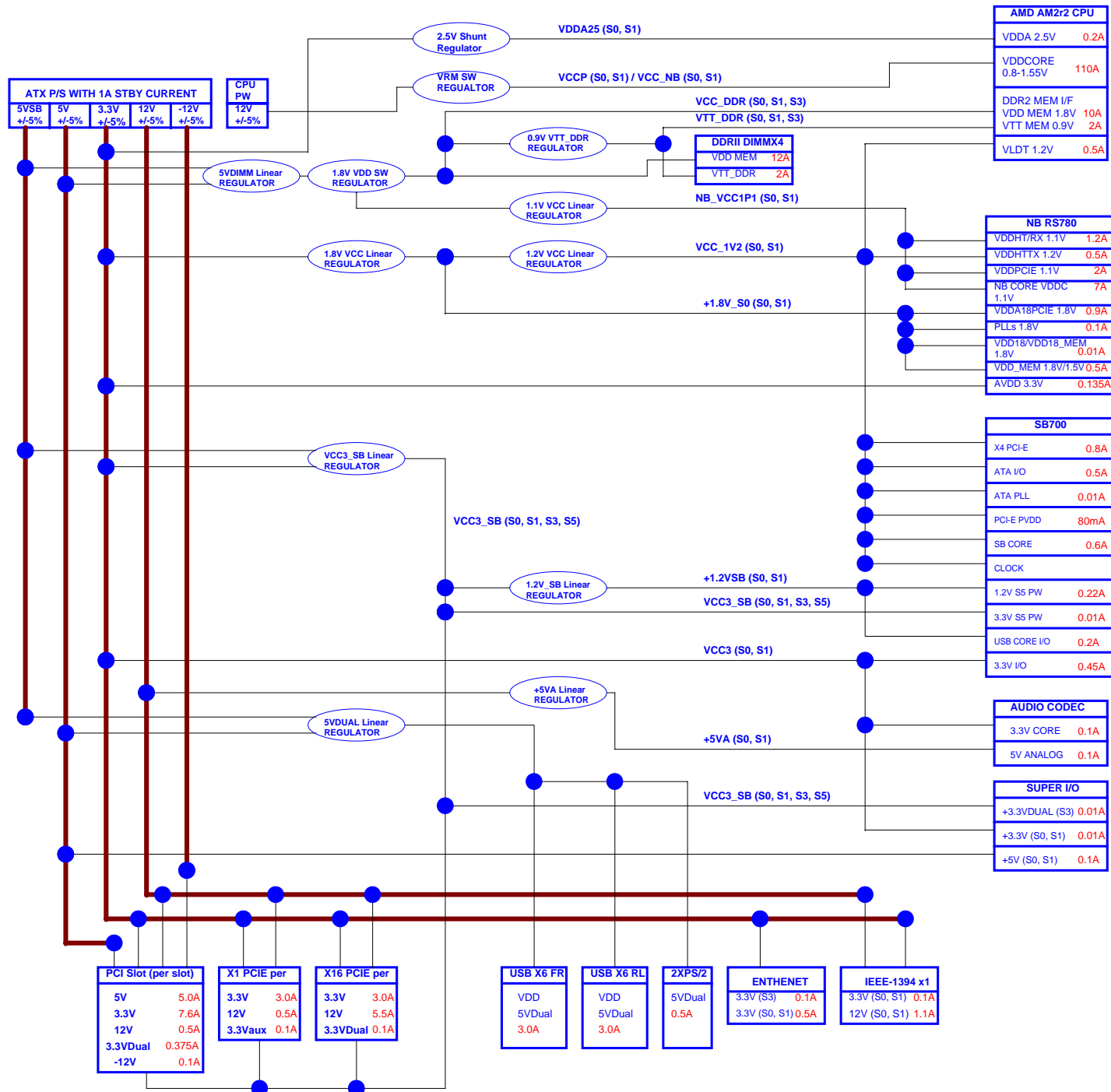
GPIO Name	Type	Function Description	Pin	Page
VID05/GP27		LEO_GPIO2	20	26
VID04/GP26		LEO_GPIO1	21	26
VID01/GP21/VGP0		LEO_GPIO0	26	26
PME#/GP54		LPC_PME#	73	26
KRST#/GP62		KBRST#	45	26
GA20/JP7		A20GATE	46	26
KDAT/GP61		KBDATA	80	26
KCLK/GP60		KBCLK	81	26
MDAT/GP57		MSDATA	82	26
MCLK/GP56		MSCLK	83	26
SUSC#/GP53		LPC_SM#	77	26
PSON#/GP42		PS_ON#	76	26
PANSWH#/GP43		PSIN	75	26
PWRON#/GP44		SB_PWRON#	72	26
PCIRST3#/GP11		ASSID_GPIO0	34	26
PCIRST2#/GP12		ASSID_GPIO1	33	26
FAN_CTL3/GP36		PWRFAN_PWM	12	26
FAN_TAC3/GP37		PWRFAN_TAC	11	26
FAN_CTL2/GP51		SYSFAN_PWM	10	26
FAN_TAC2/GP52		SYSFAN_TAC	9	26
FAN_CTL1		CPUFAN_PWM	8	26
FAN_TAC1		CPUFAN_TAC	7	26
VID2/GP32		COM_GPIO2	17	26
VID3/GP33		FUSB_G1	16	26
VID4/GP34		FUSB_G2	14	26
VID5/GP35		FUSB_G3	13	26

DEVICE	MCP1 INT Pin	REQ#/GNT#	IDSEL	CLOCK
PCI Slot 1	PCI_INTA# PCI_INTB# PCI_INTC# PCI_INTD#	REQ#0 PGNT#0	AD16	PCICK0
PCI Slot 2	PCI_INTB# PCI_INTC# PCI_INTD# PCI_INTA#	REQ#1 PGNT#1	AD17	PCICK1
IEEE-1394	PCI_INTC#	REQ#2 PGNT#2	AD18	PCICK2

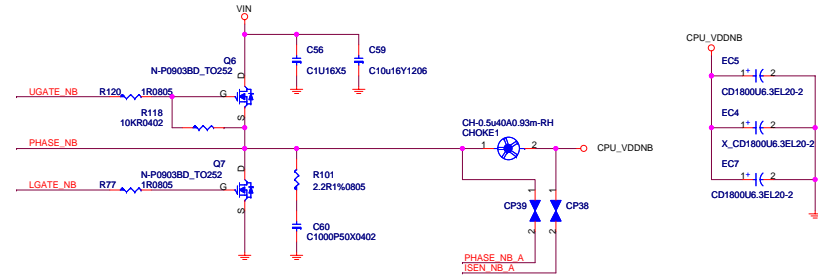
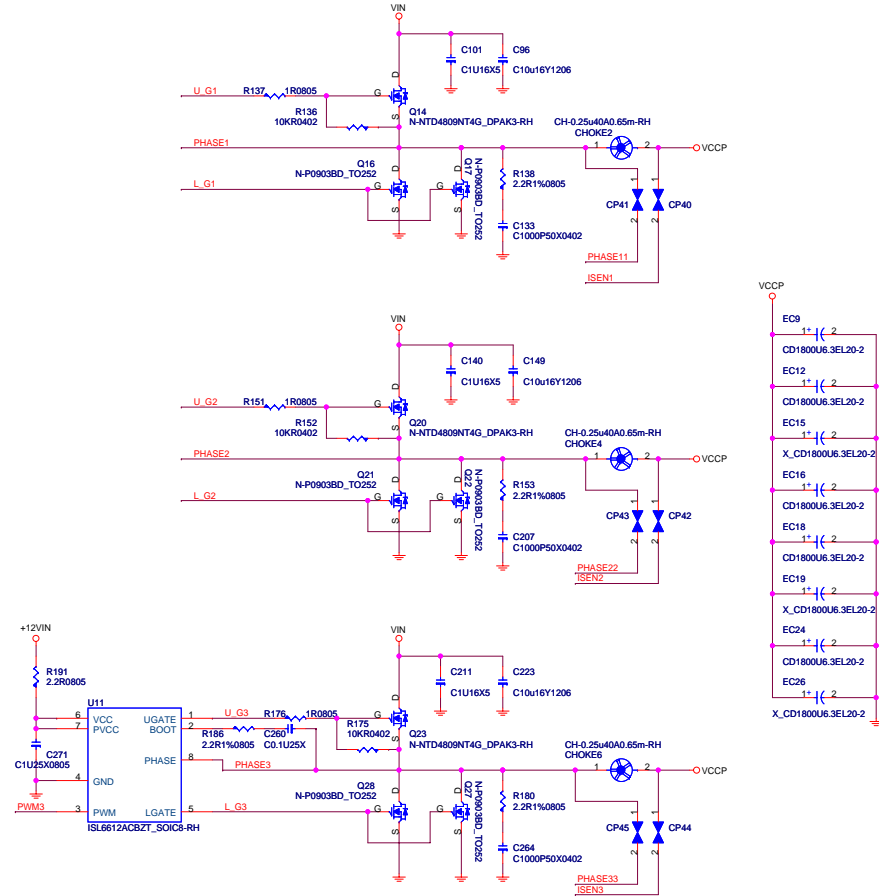
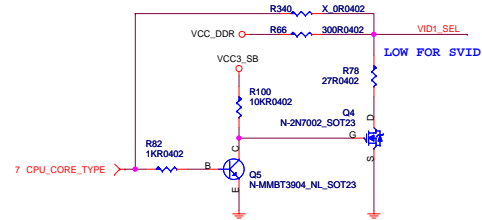
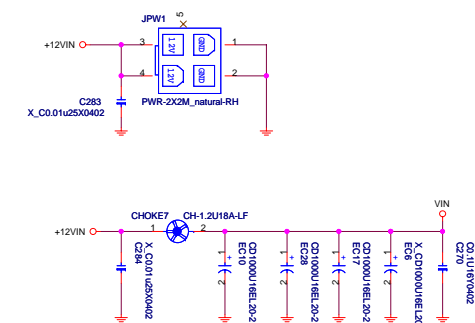
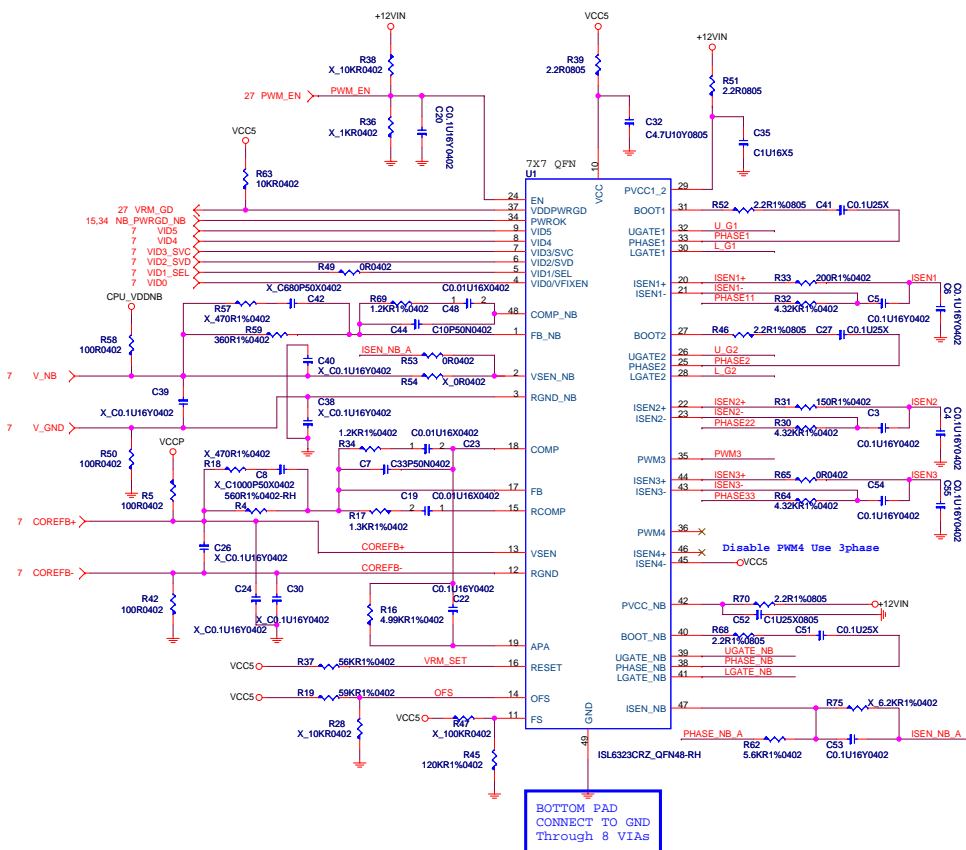


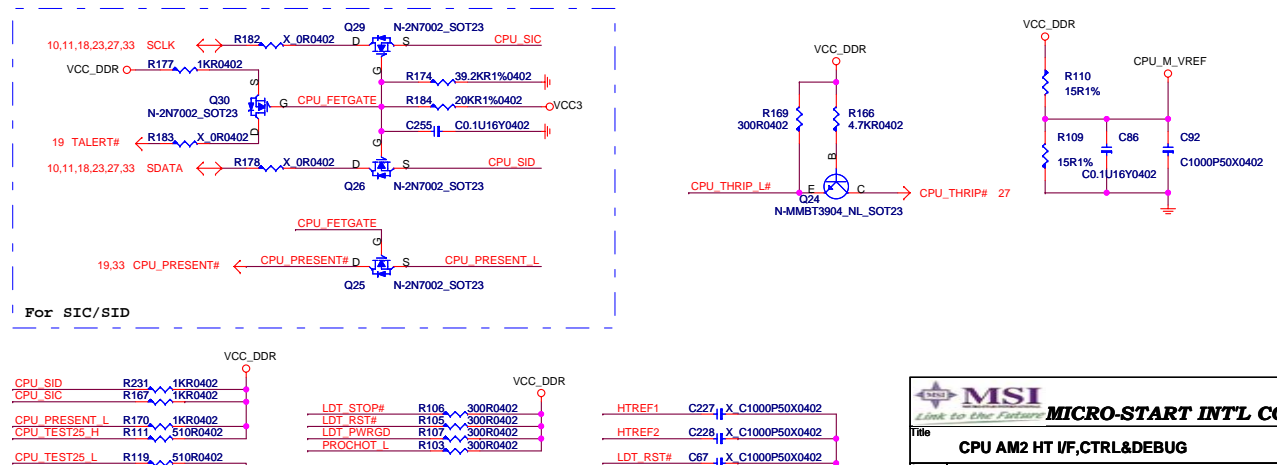
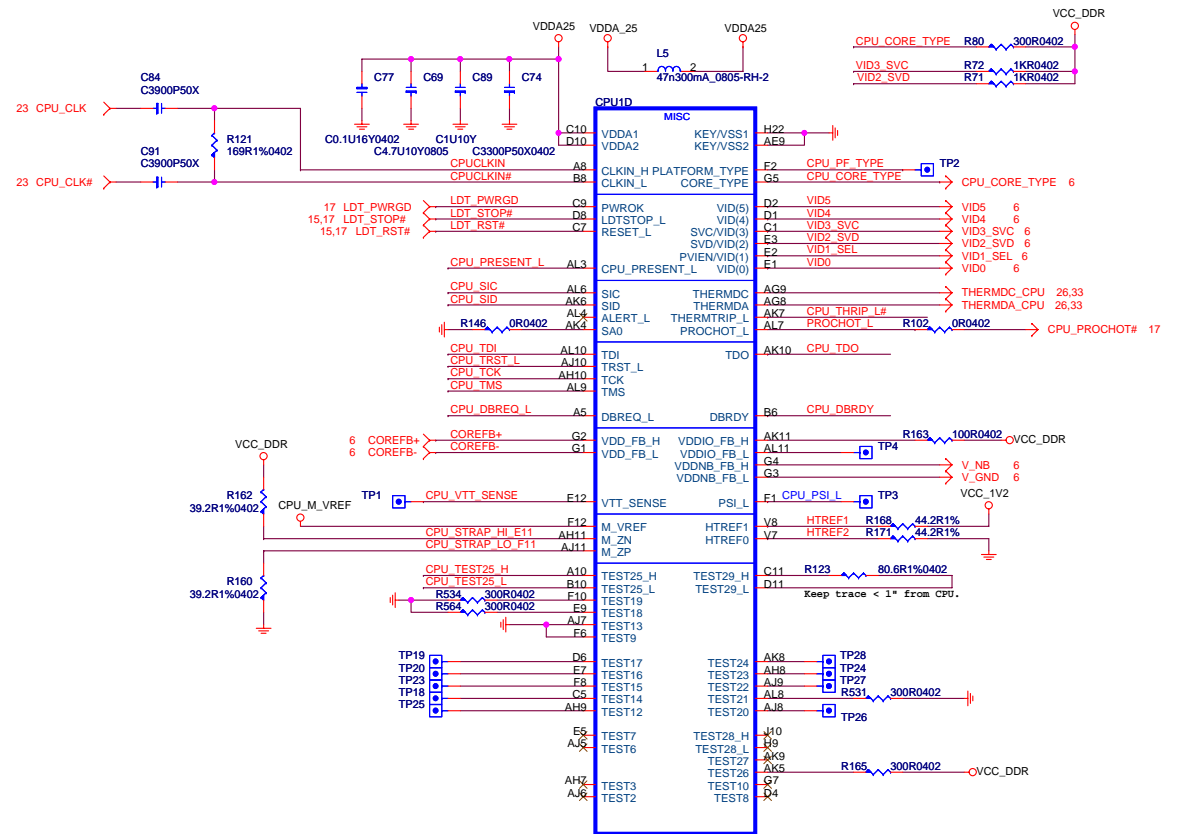
External clock mode
Internal clock mode

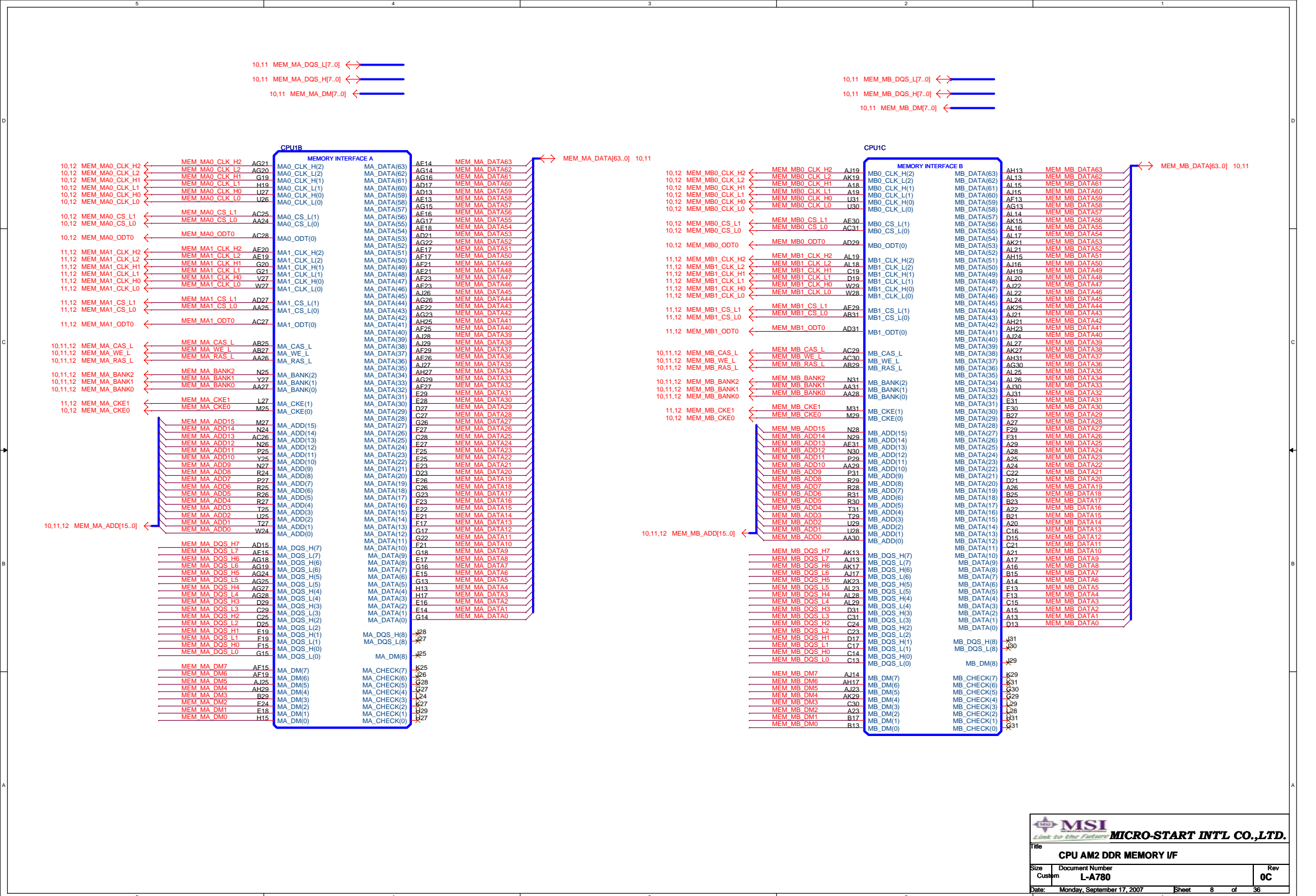
Power Deliver Chart



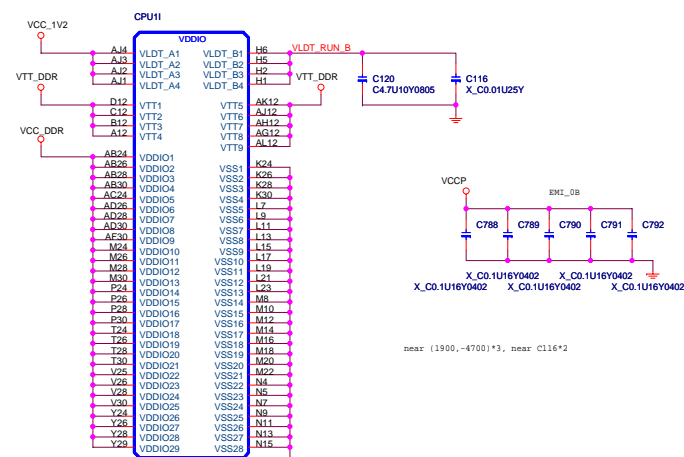
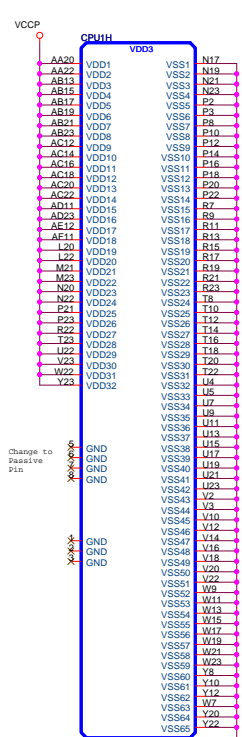
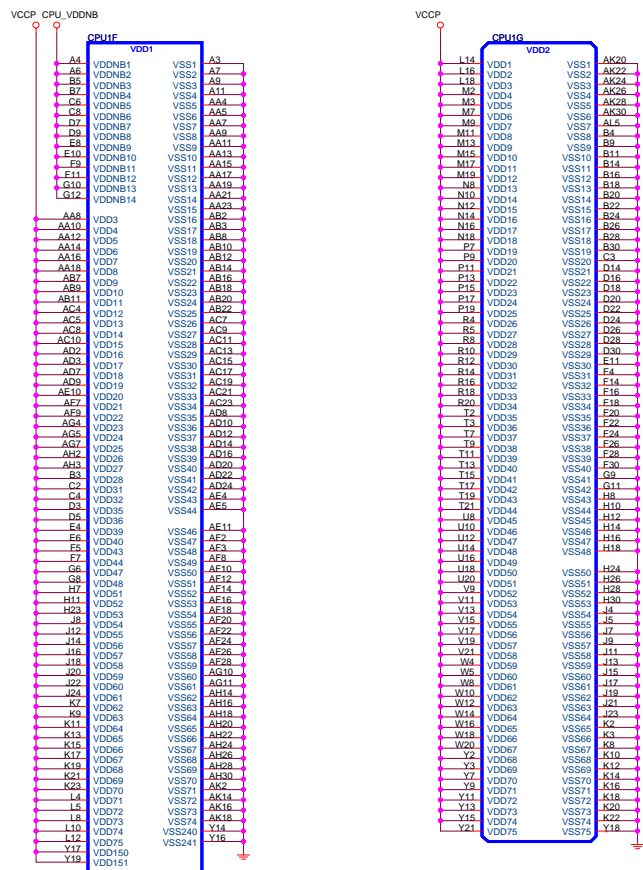
Intersil 6323 3 Phase



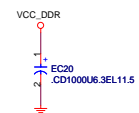
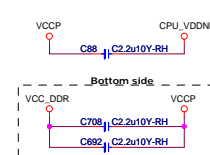
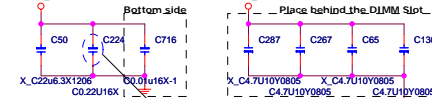
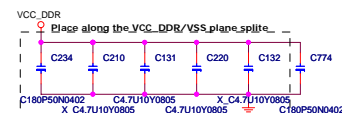
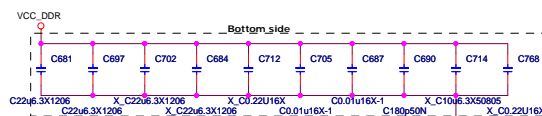
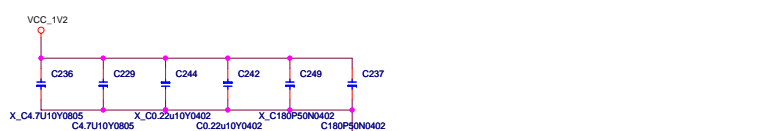
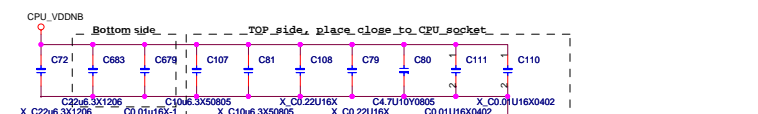
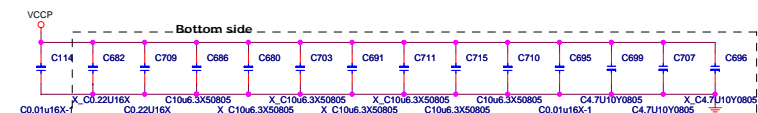
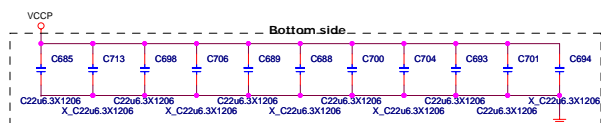




CPU AM2 PWR & GND

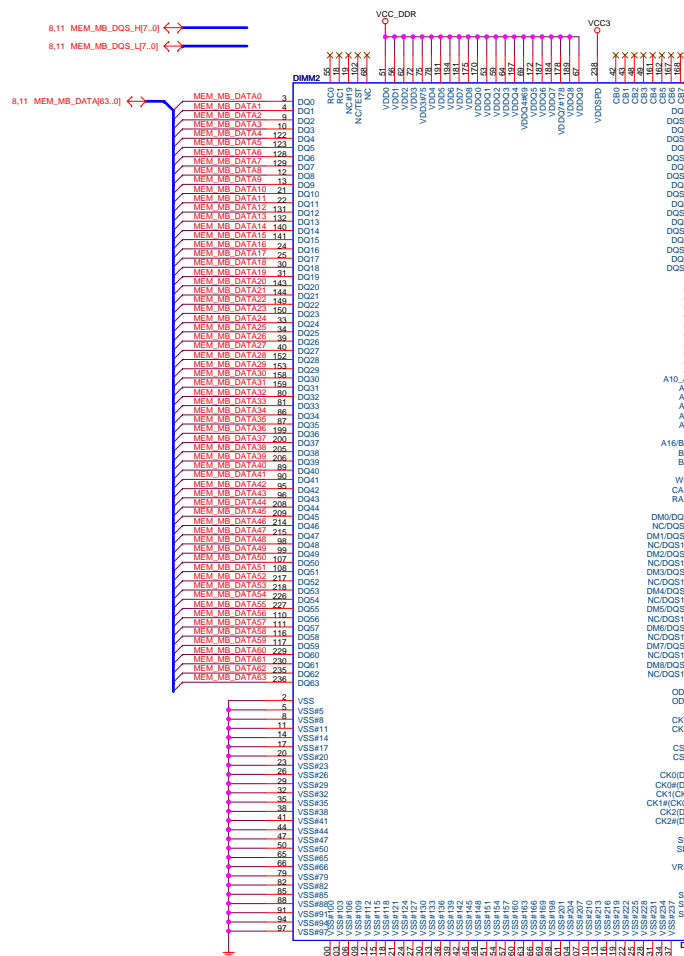
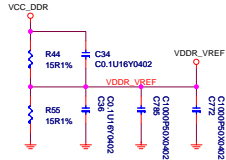


near (1900,-4700)*3. near C116*2

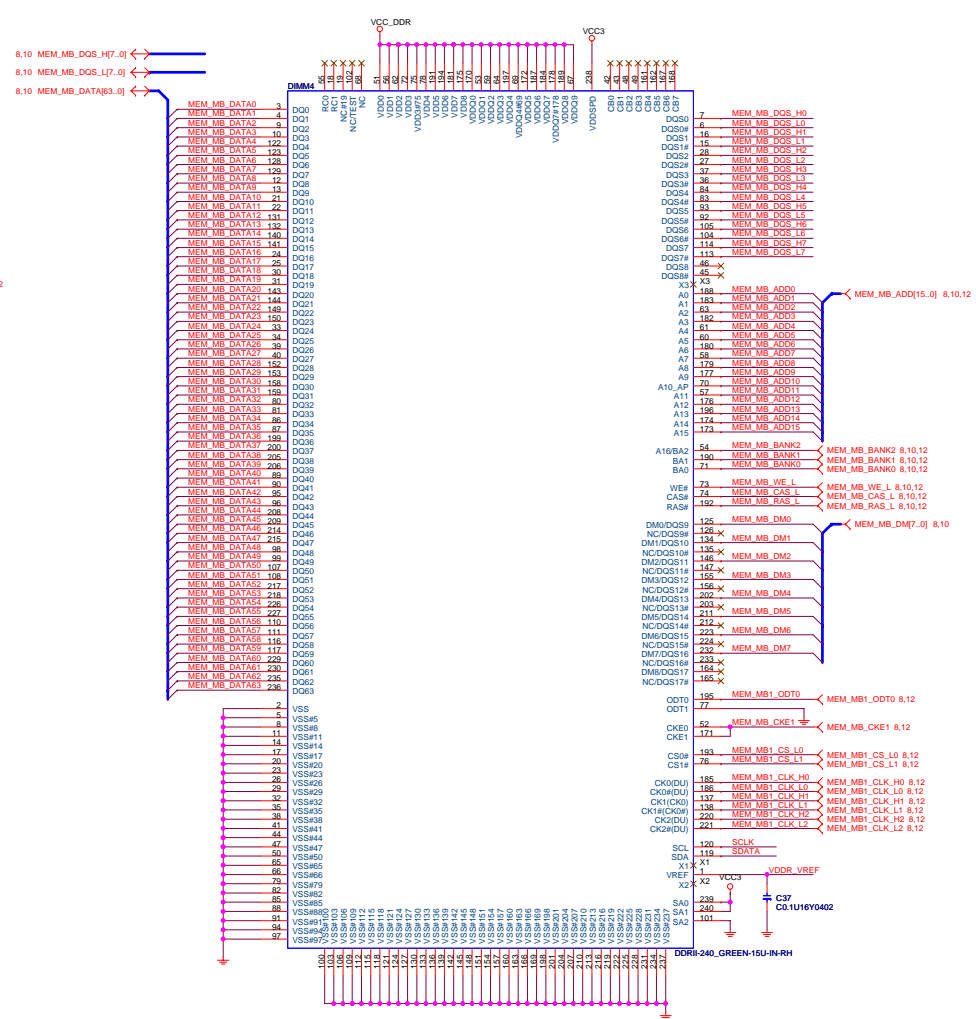
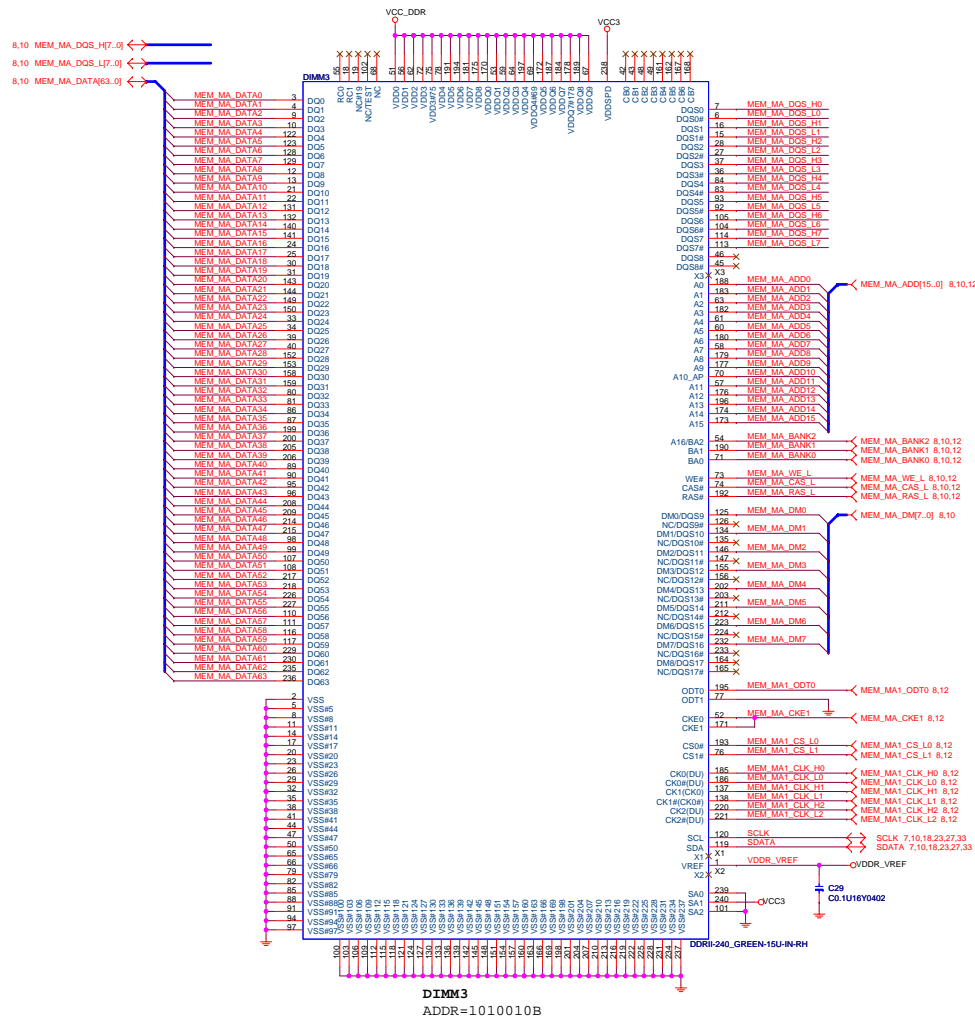


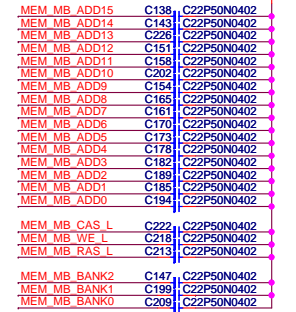
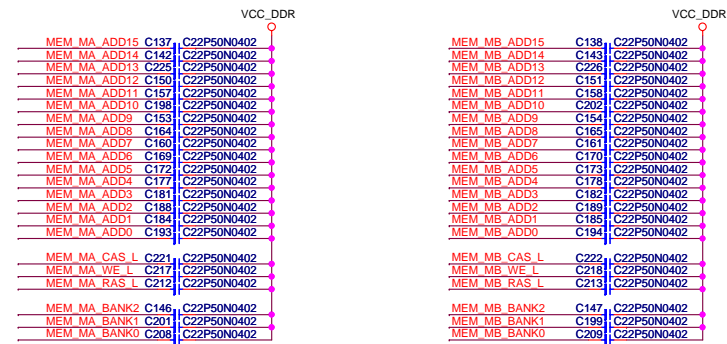
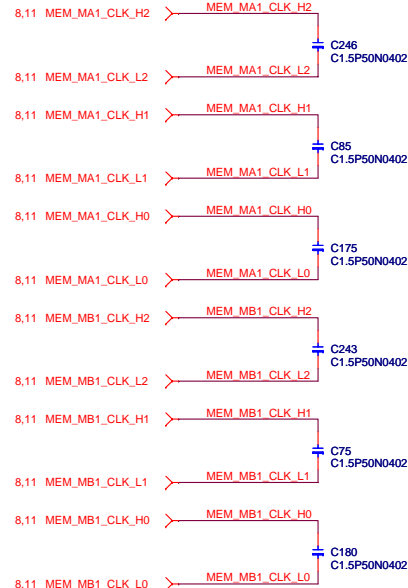
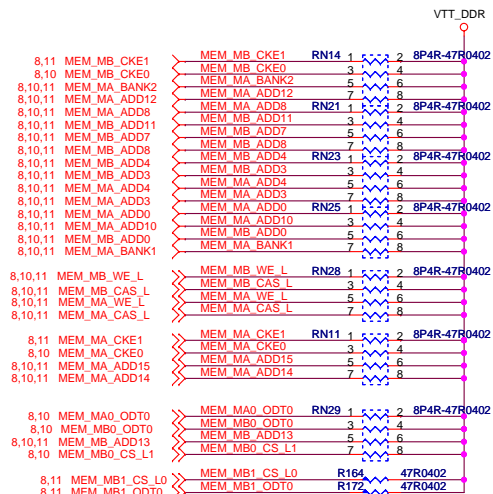
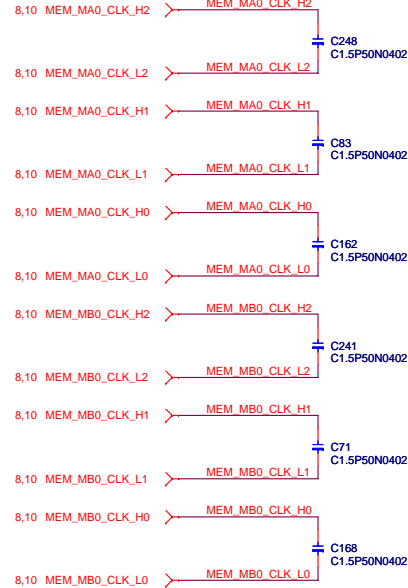
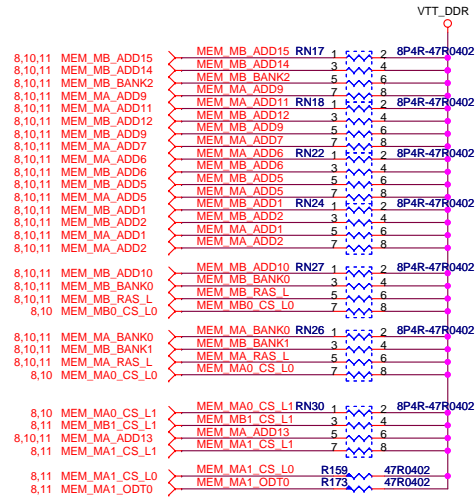


DIMM 1
ADDR=1010000B



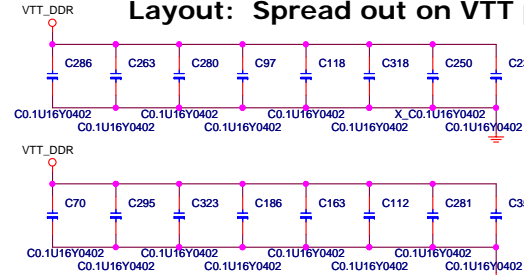
DIMM 2
ADDR=1010001B



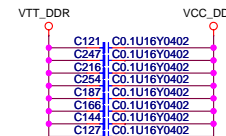
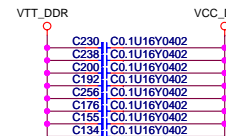
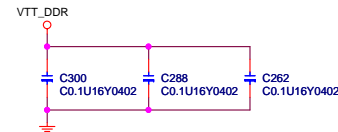
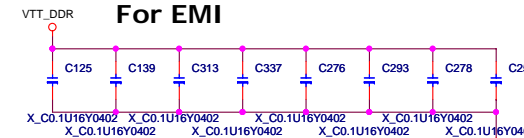


Decoupling Between Processor and DIMMs

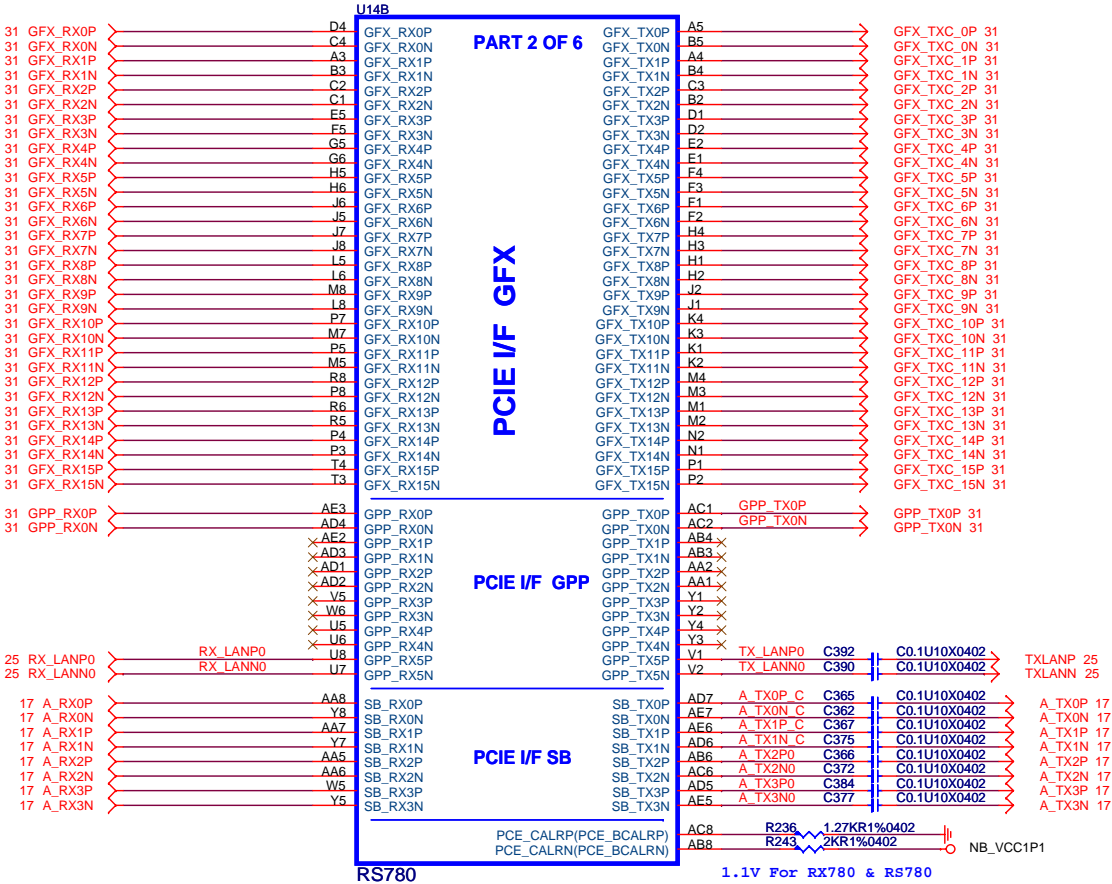
Layout: Spread out on VTT pour

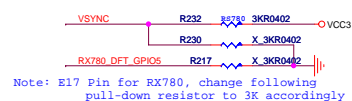
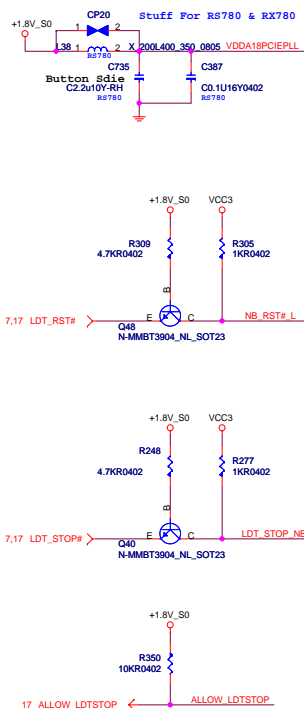
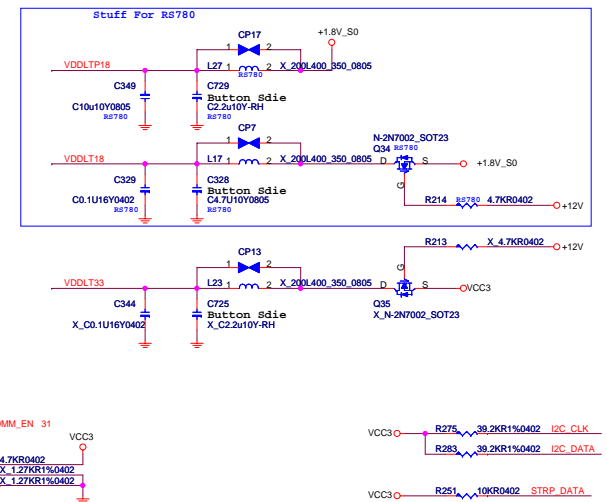


For EMI



RS780-PCIE I/F

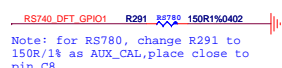


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Note: E17 Pin for RX780, change following pull-down resistor to 3K accordingly

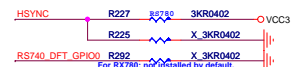


Note: for RX780, change following pull-down resistor to 3K accordingly



Note: for RX780, R1221
(RX780_DFT_GPIO1) to 3K accordingly

Note: for RX780, R1221
(RX780_DFT_GPIO1) to 3K accordingly



RS740 DFT GPIO0 R292 X 3KR040
For RX780: not installed by default

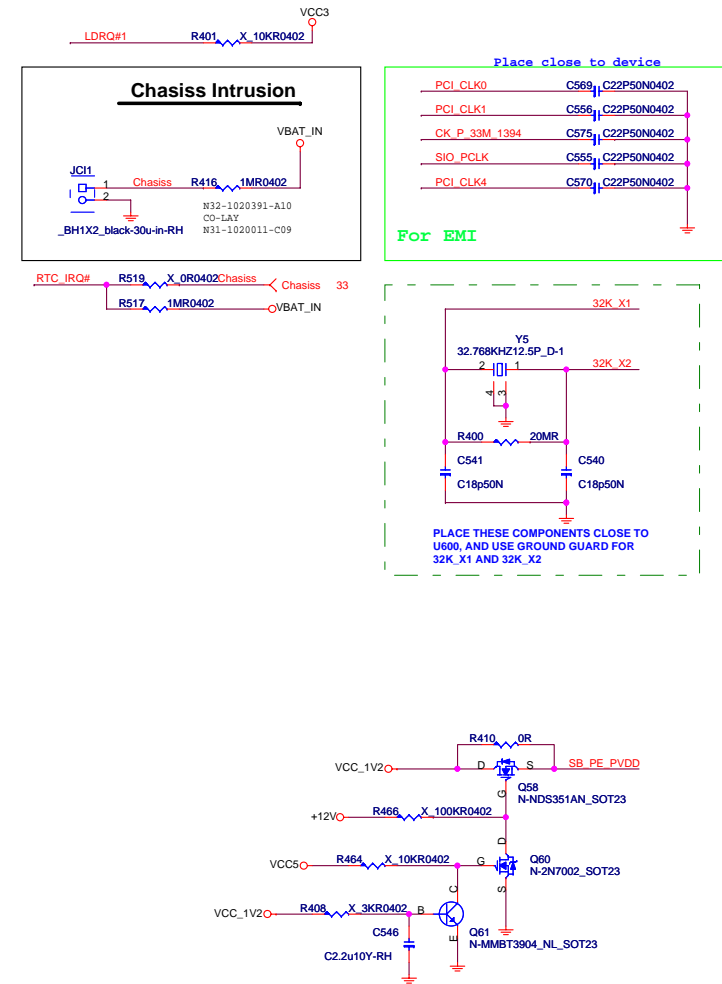
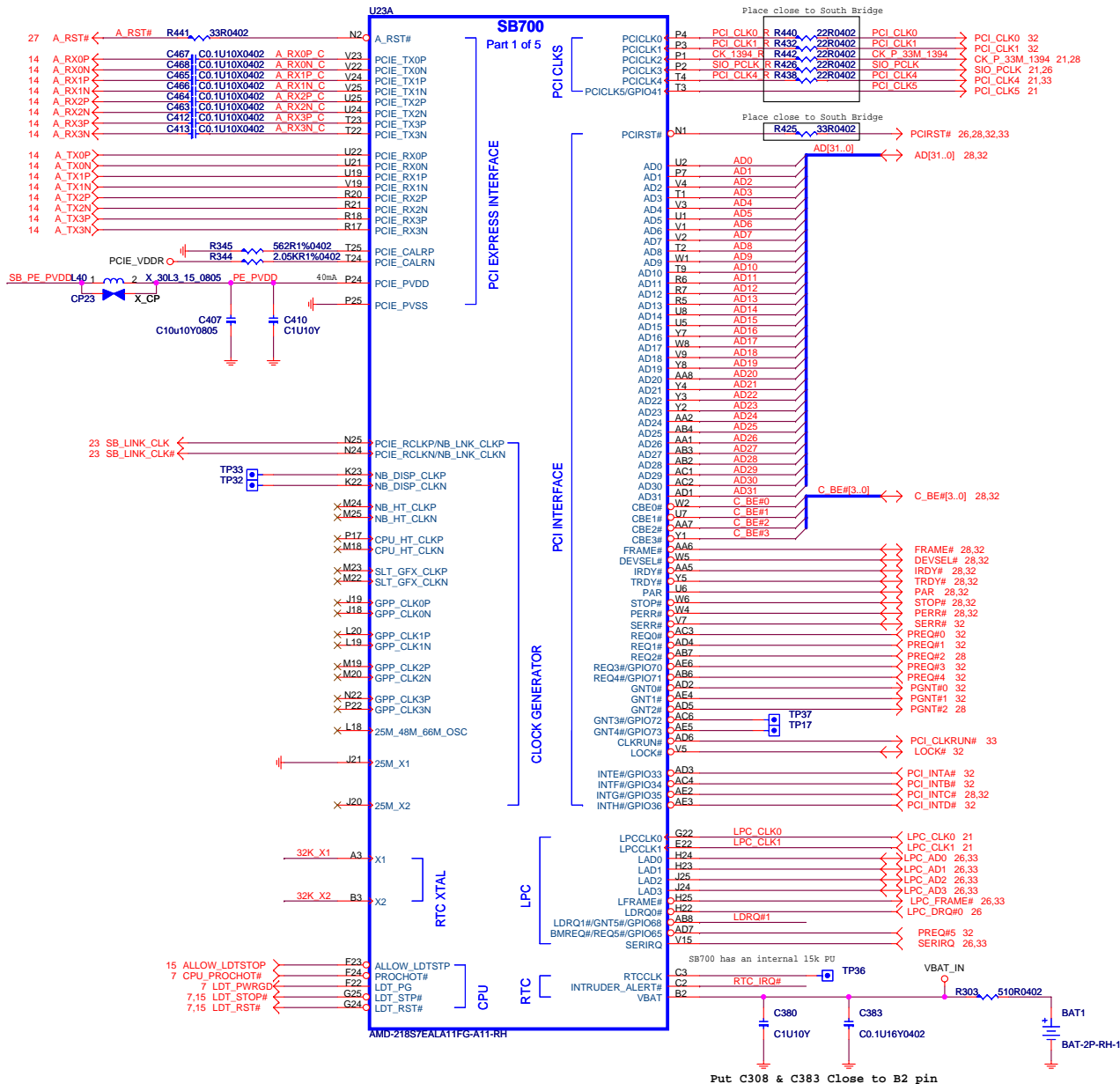
```
Enables the Test Debug Bus using GPIO and/or memory IC
1 : Disable (RS740); Enable (RX780/RS780)
0 : Enable (RS740); Disable(RX780/RS780)
RS740: pin DFT_GPIO5
RX780: pin DFT_GPIO5
RS780: pin VSYNC
```

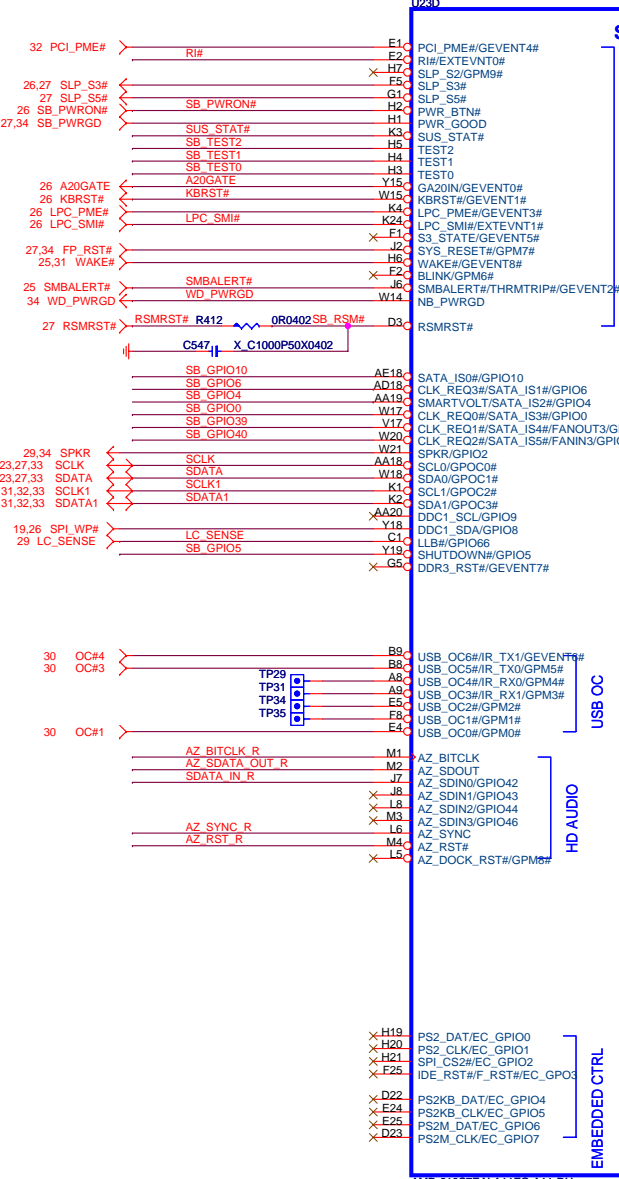
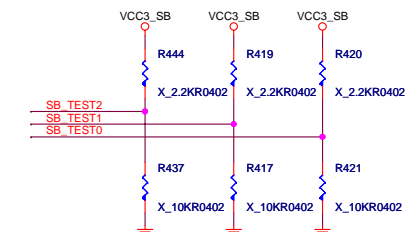
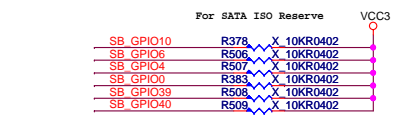
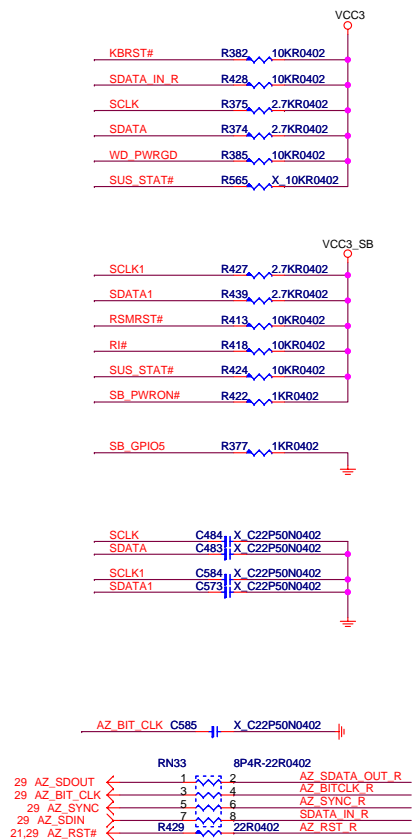
```
These pin straps are used to configure PCI-E GPP mode.
111: register defined (register default to Config E)    default
110: 4-0-0-0-0    Config A
101: 4-4-0-0-0    Config B
100: 4-2-2-0-0    Config C
011: 4-2-1-1-0    Config D
010: 4-1-1-1-1    Config E
others: register defined (default to Config E)
```

```
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use
  default values if not connected
RS740: pin DFT_GPIO1
RX780: pin DFT_GPIO1
RS780: pin SUS_STAT#
```

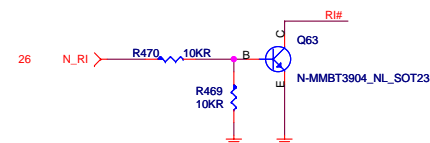
```
Enables Side port memory
1. Disable (RS740/RS780)
0 : Enable (RS740/RS780)
RS740: pin DFT_GPIO0
RS780: pin HSYNC
RX780: Not Applicable
```

	RX780	RS740	RS780
DEBUG_OUT0	RED(DFT_GPI0)	LVDS_DIGON	LVDS_DIGON
DEBUG_OUT1	GREEN(DFT_GPI01)	LVDS_ENA_BL	LVDS_ENA_BL
DEBUG_OUT2	Y(DFT_GPI02)	LVDS_BLDN	LVDS_BLDN
DEBUG_OUT3	BLUE(DFT_GPI03)	TMDS_HPD	TMDS_HPD
DEBUG_OUT4	TXOUT_L2N(DBG_GPI00)	X	AUX1N
DEBUG_OUT5	TXCLK_LP(DBG_GPI01)	X	AUX1P
DEBUG_OUT6	TXOUT_L3N(DBG_GPI02)	X	HPD
DEBUG_OUT7	TXCLK_LN(DBG_GPI03)	X	AUX_CAL

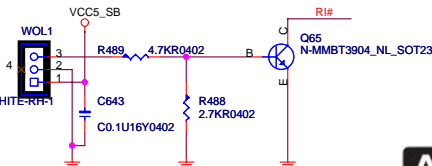




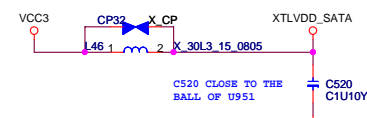
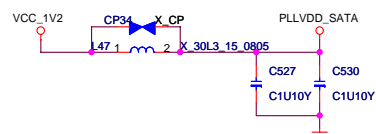
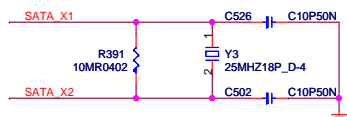
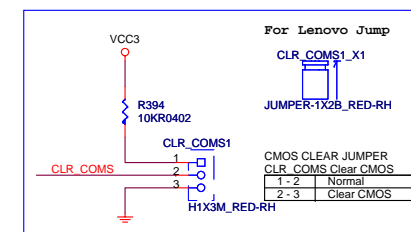
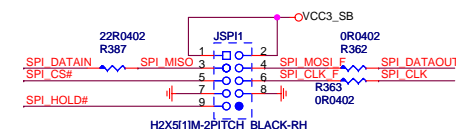
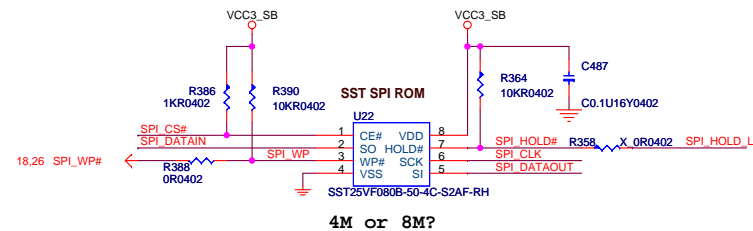
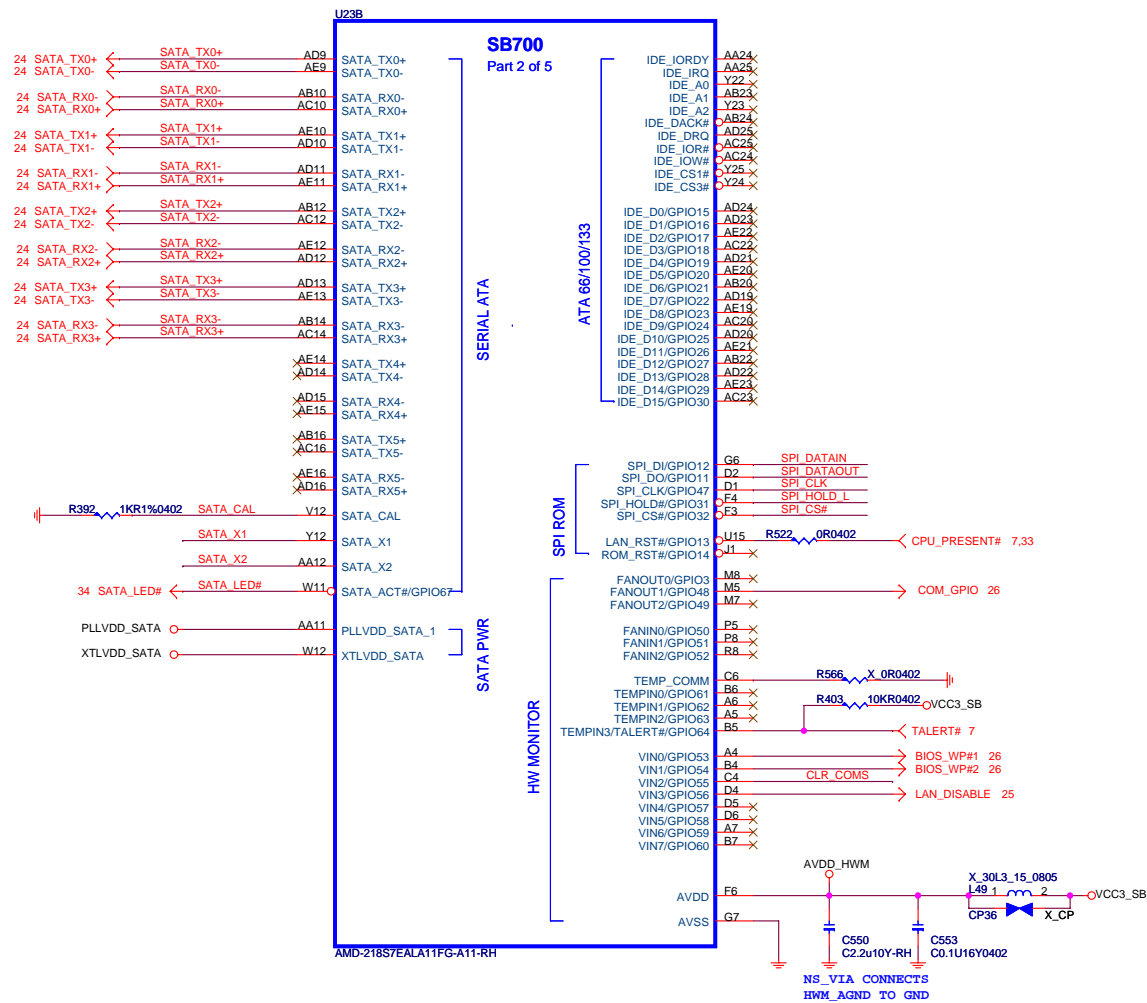
Wake On Modem Header

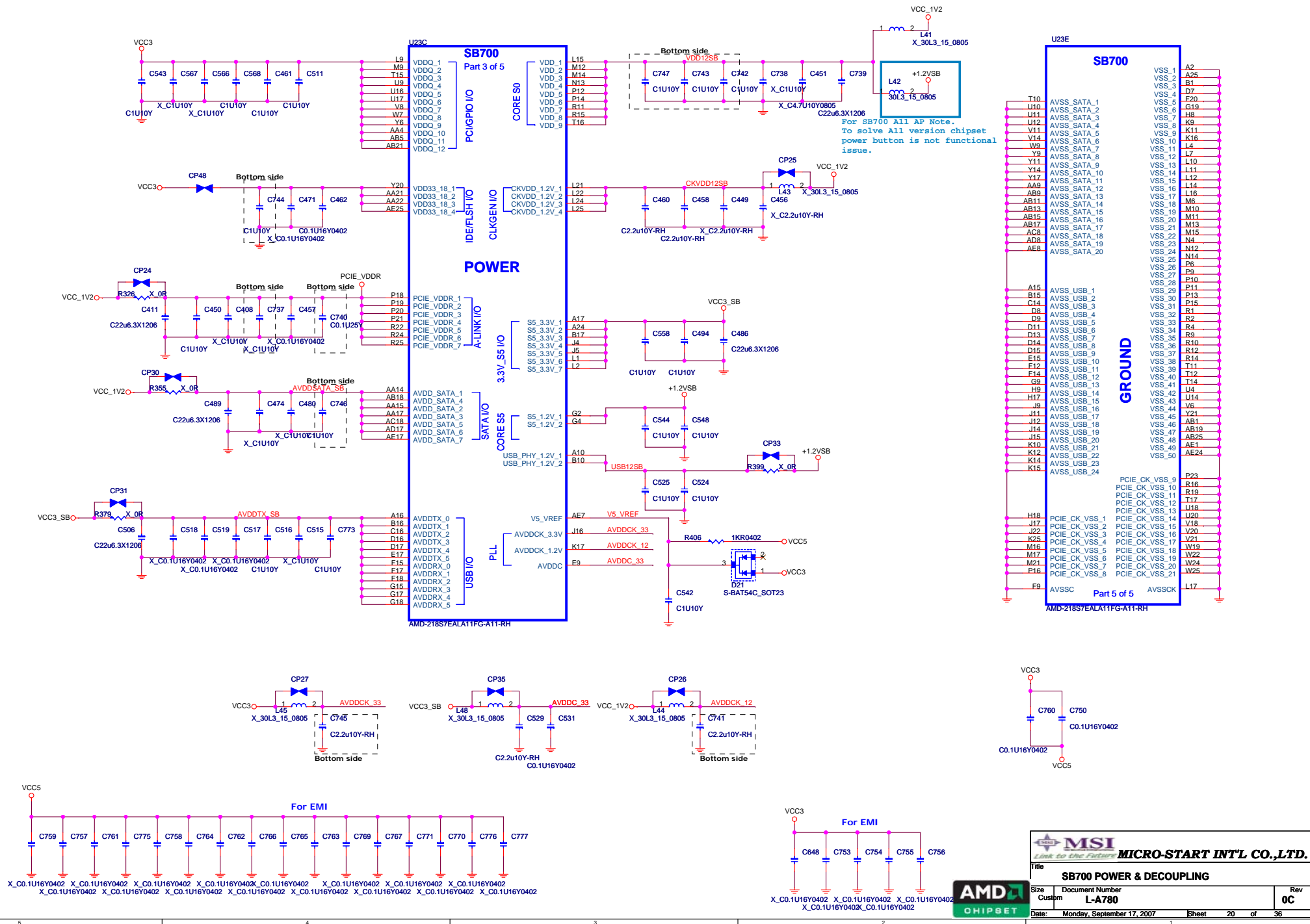


Wake on LAN



USB11 FRONT PANEL
USB10 FRONT PANEL
USB9 FRONT PANEL
USB8 FRONT PANEL
USB7 FRONT PANEL
USB6 FRONT PANEL
USB5 STACK4 USB4
USB4 STACK4 USB3
USB3 STACK4 USB2
USB2 STACK4 USB1
USB1 LAN USB BOTTOM
USB0 LAN USB TOP

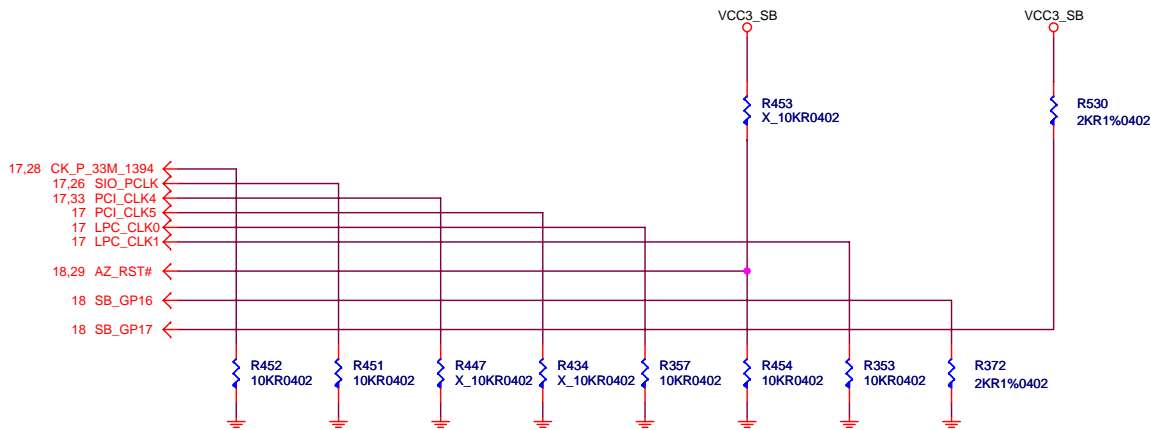







REQUIRED STRAPS

SB600 HAS 15K INTERNAL PD FOR AC_SDATA_OUT,
15K PU FOR RTC_CLK, EXTERNAL PU/PD IS
NOT REQUIRED; FOR SB460, EXTERNAL PU/PD ARE
REQUIRED



	PCI_CLK2 CK_P_33M_1394	PCI_CLK3 SIO_PCLK	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#	GP17 GP16	
	Watchdog timer on NB_PWGRD	Debug straps	TPM CLOCK	RESERVED	Booting from PCI Memory	Internal Clock Generator	INTERNAL RTC	EC ENABLED	ROM TYPE: NC, NC = Reserved NC, L = SPI ROM DEFAULT L, NC = LPC ROM L, L = FWH ROM	
PULL HIGH	ENABLED (VCC3)	ENABLED (VCC3)			ENABLED (VCC3_SB)	ENABLED (VCC3_SB)		ENABLED	Note: NC represents internal 10-k? 5% pull-up	
PULL LOW	DISABLED DEFAULT	DISABLED DEFAULT			DISABLED DEFAULT	DISABLED DEFAULT	NC IS EXT. RTC DEFAULT	DISABLED DEFAULT		



MICRO-START INTL CO.,LTD.

Title

SB700 STRAPS

Size B

Document Number

Rev

L-A780

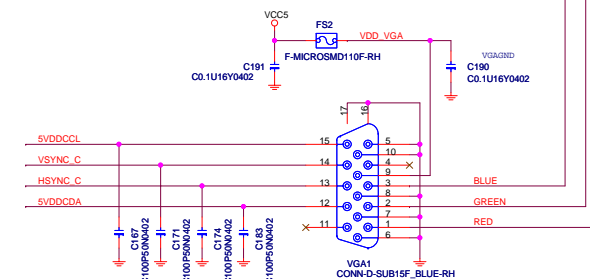
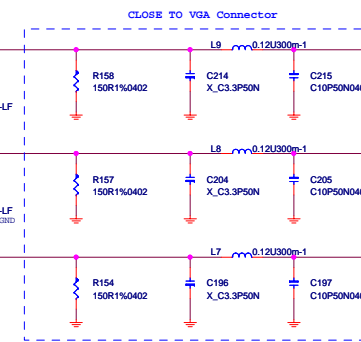
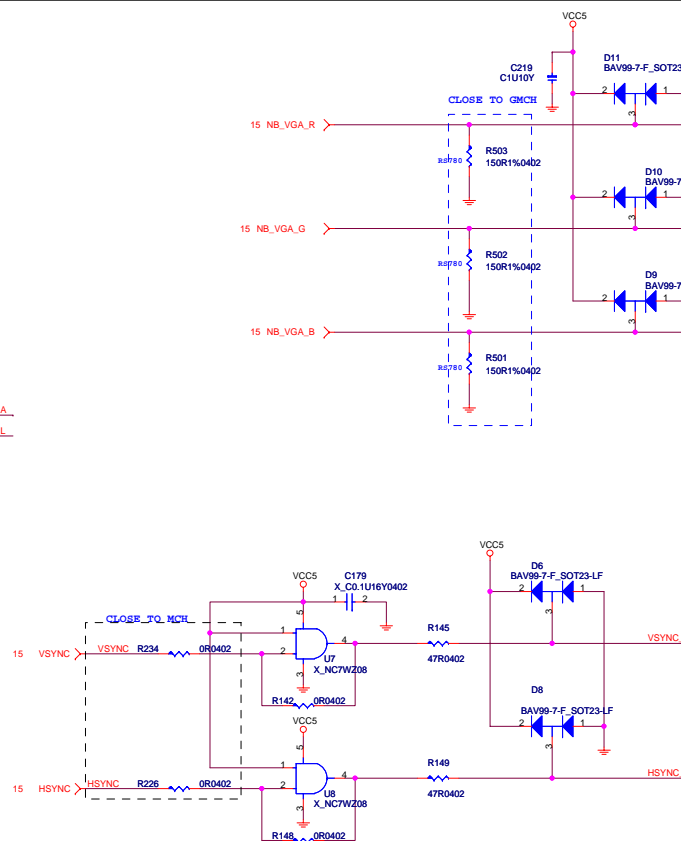
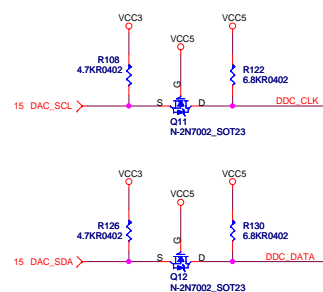
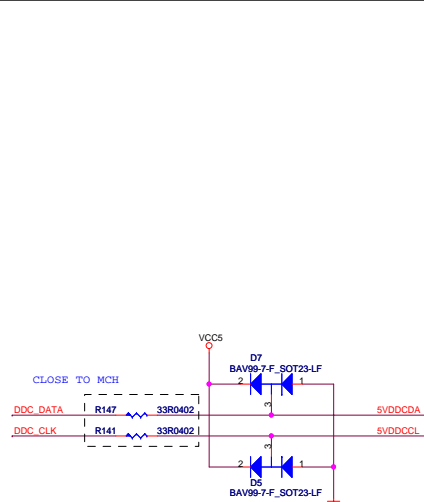
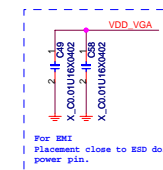
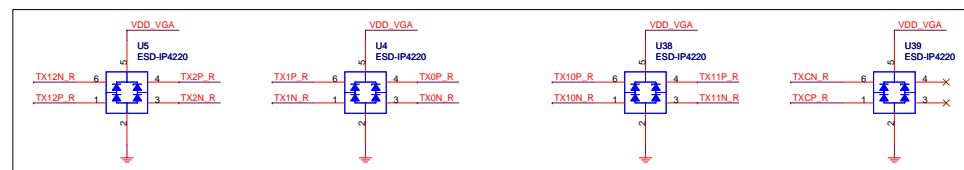
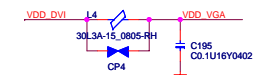
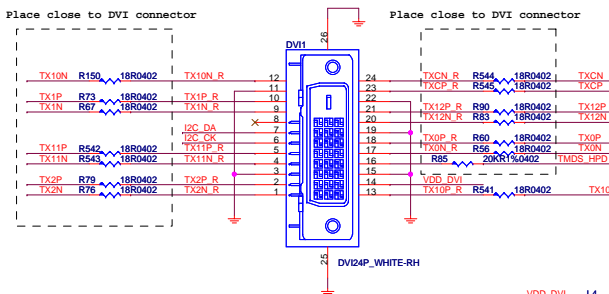
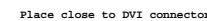
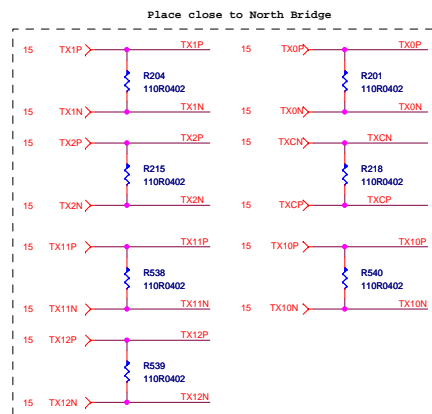
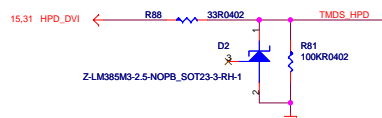
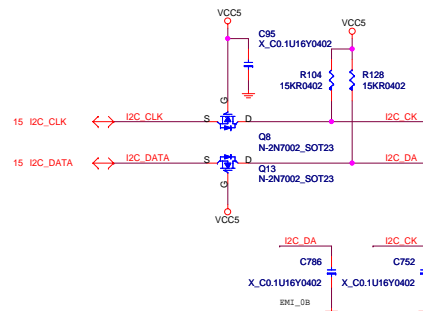
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Date: Monday, September 17, 2007

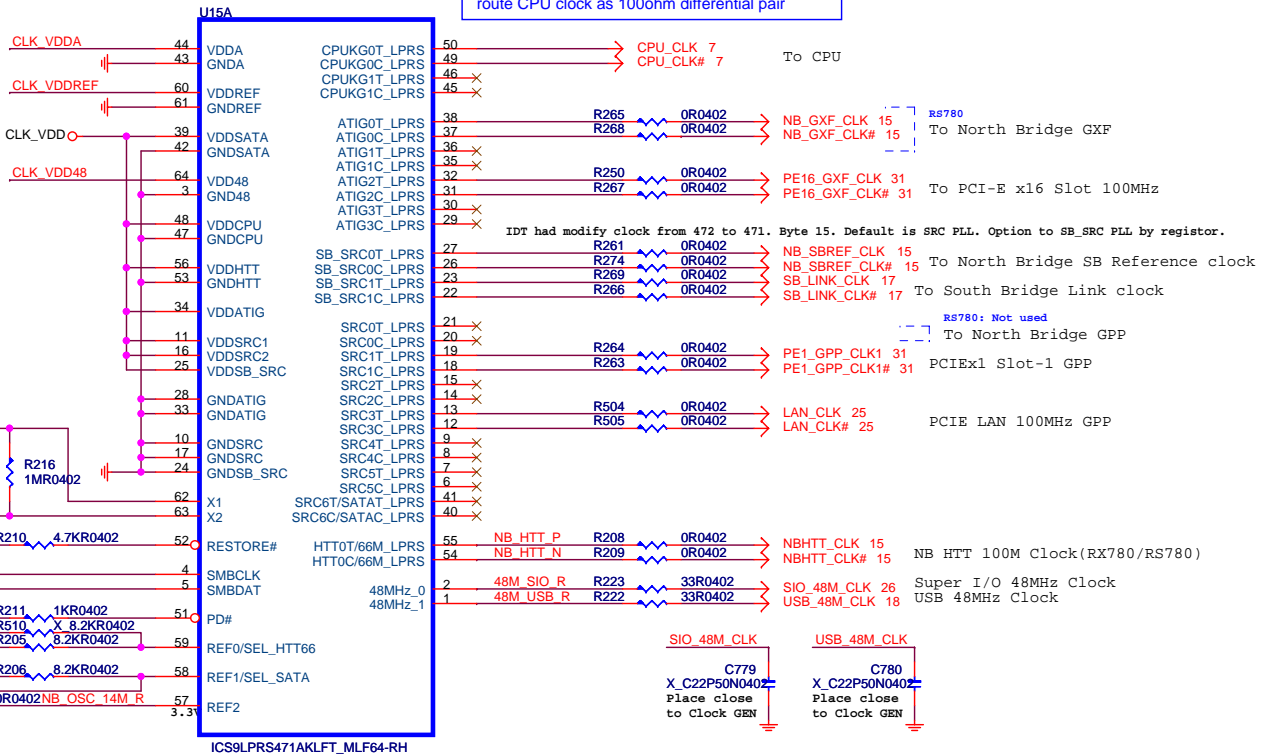
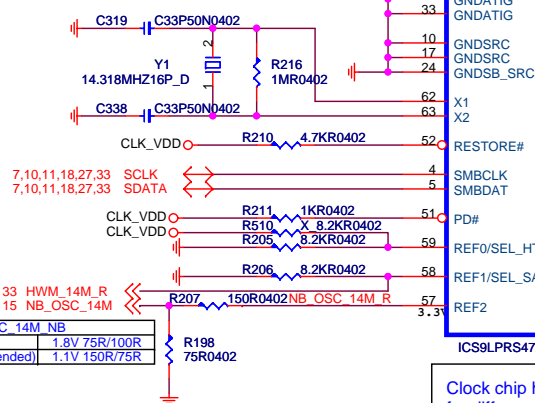
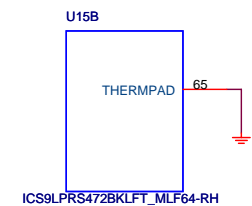
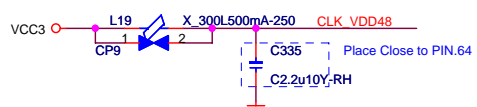
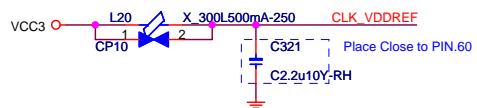
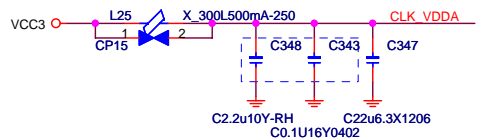
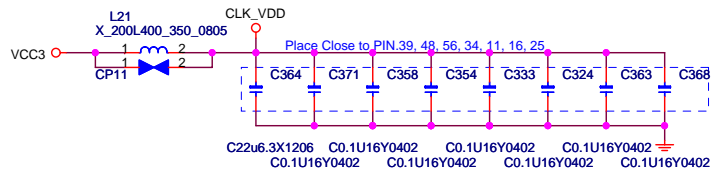
Sheet 21 of 36



DVI CONNECTOR



Clock Gen ICS9LPR472



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.

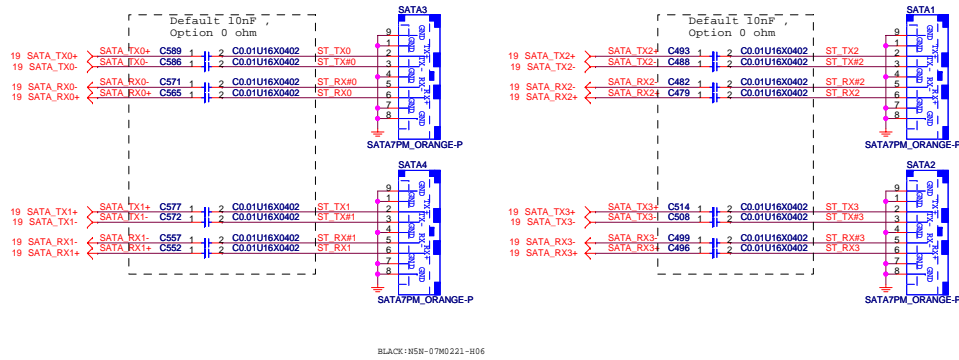
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780	
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF	
HT_REFCLKN	NC	100M DIFF	100M DIFF	
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)	100M DIFF
REFCLK_N	NC	NC	vref	100M DIFF
GF_X_REFCLK	100M DIFF	100M DIFF	100M DIFF(IN/OUT)*	
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)	
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF	

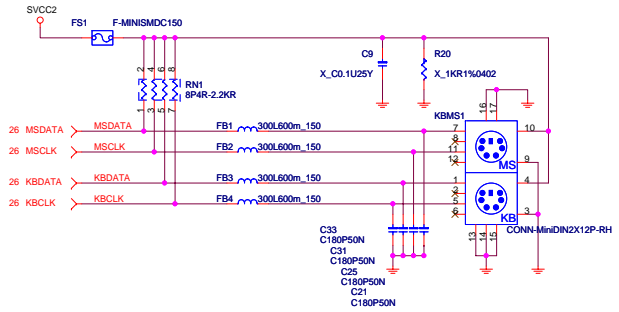
* RS780 can be used as clock buffer to output two PCIE reference clocks
By default, chip will be configured as input mode, BIOS can program it to output mode.

REF0/SEL_HTT66	HTT CLOCK	REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL	0	100.00 DIFFERENTIAL SPREADING SRC CLCOK
1	66.66 SINGLE END	1	100.00 NON-SPREADING DIFFERENTIAL SATA CLCOK

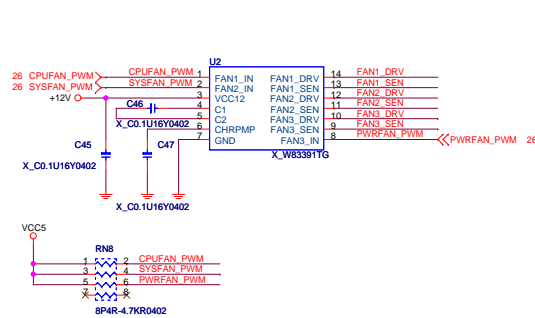
SERIAL ATA CONNECTOR BLOCK



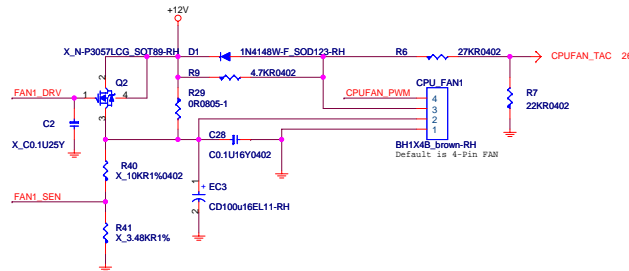
PS2 KEYBOARD & MOUSE CONNECTOR



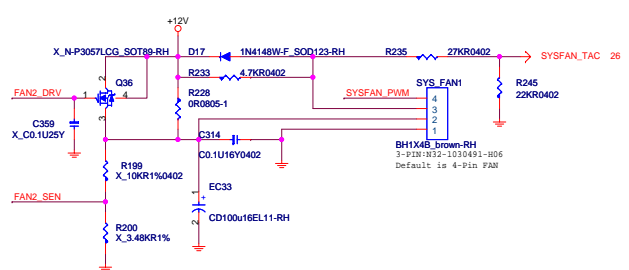
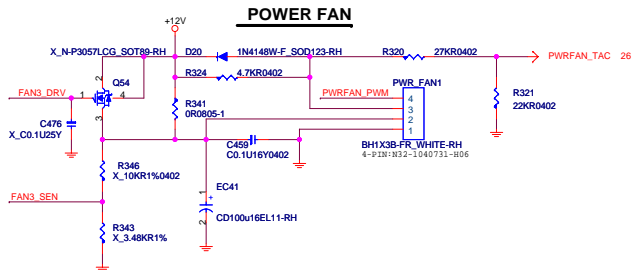
PWM FAN CONTROL



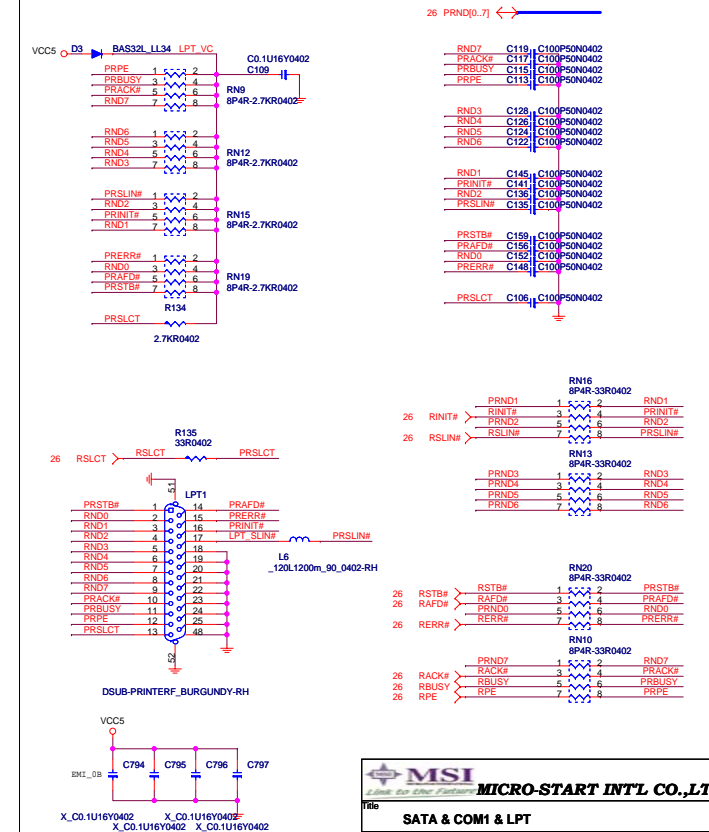
CPU FAN



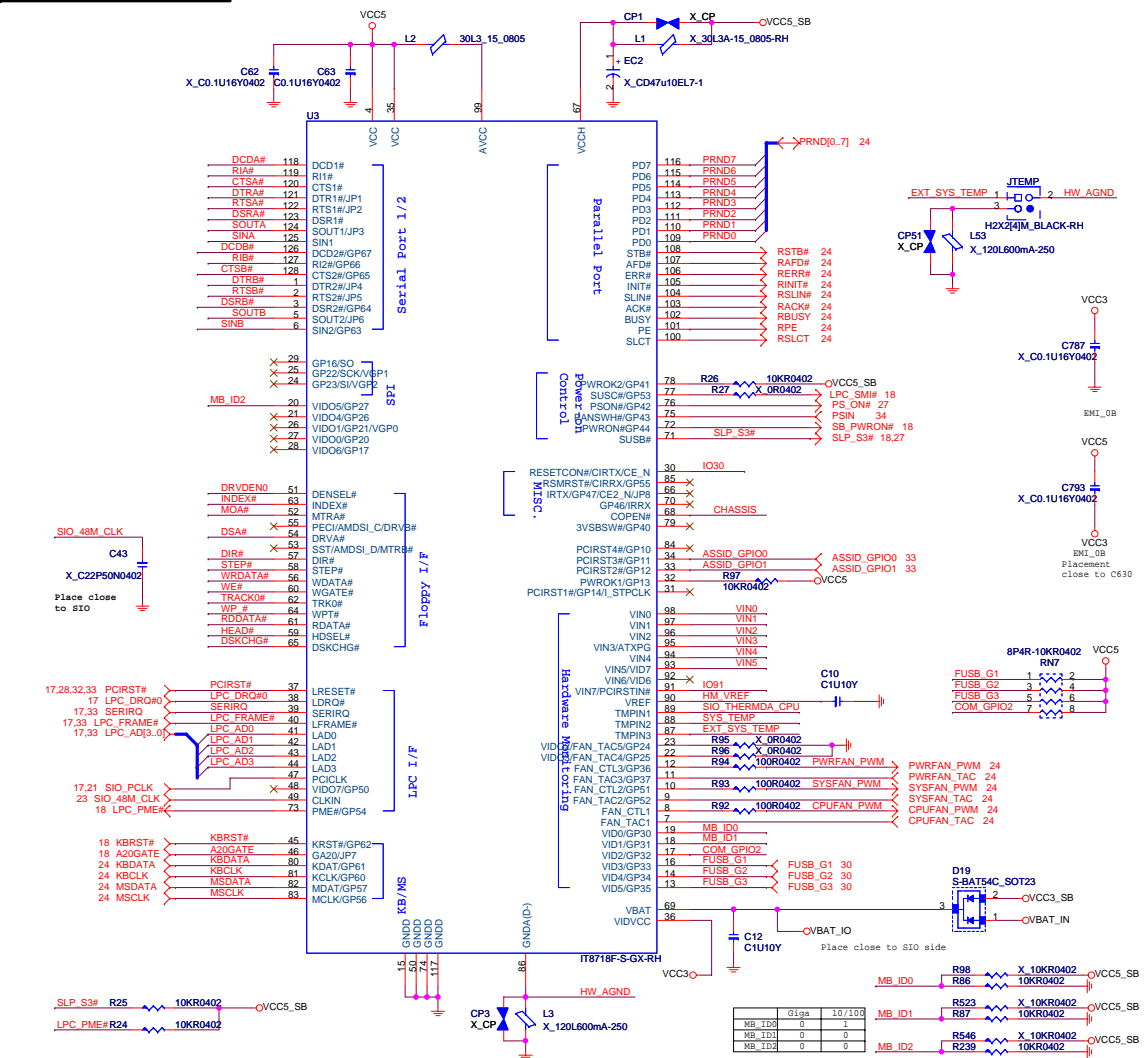
SYSTEM FAN



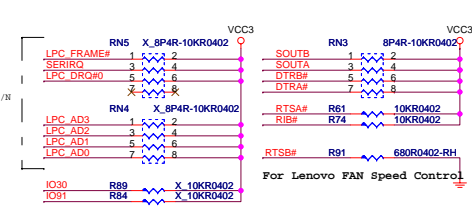
PARALLAL PORT



LPC I/O IT8718F



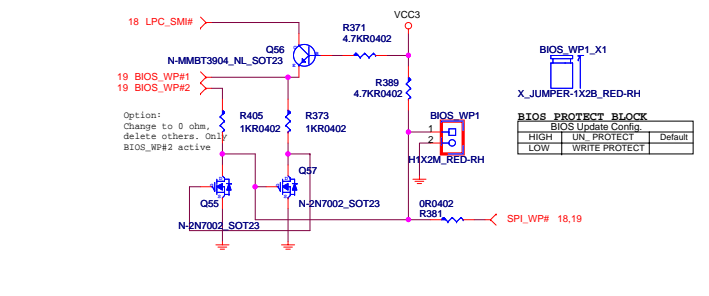
SUPER I/O STRAPPING RESISTOR



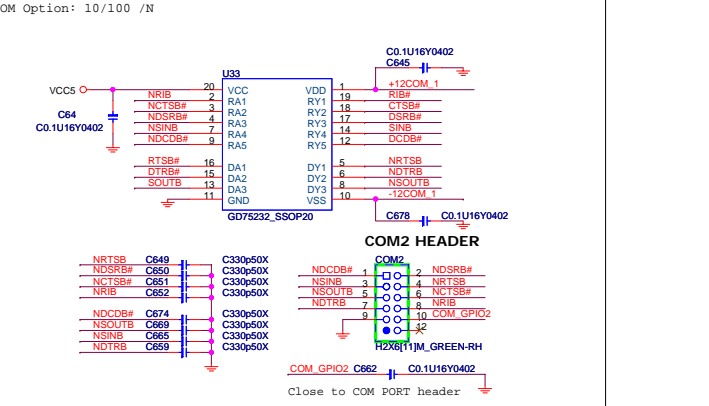
Power On Strapping Options

Symbol	value	Description
Flashseg1_EN	1	Disabled.
VIDO_SEL	0	Flash I/F Address Segment 1 (FFFF_0000h-FFFF_FFFFh, 000F_0000h-000F_FFFFh) is enabled
VIDO_SEL	1	Disable VIDOOUT pins(except VIDO6 & VIDO7)
CHIP_SEL	0	Enable VIDOOUT pins
CHIP_SEL	...	Chip selection in configuration.
BUF_SEL	1	The output buffers of PCIRST1#, PCIRST2#, PCIRST3#, PCIRST4# are open-drain.
BUF_SEL	0	The output buffers are push-pull.
FAN_CTL_SEL	1	The default value of EC Index 15h / 16h / 17h is 00h
FAN_CTL_SEL	0	The default value of EC Index 15h / 16h / 17h is 40h
VID_ISEL	1	The threshold voltage of VID is 2.0 / 0.8V
VID_ISEL	0	The threshold voltage of VID is 0.8 / 0.4V

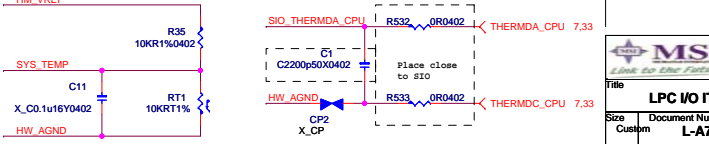
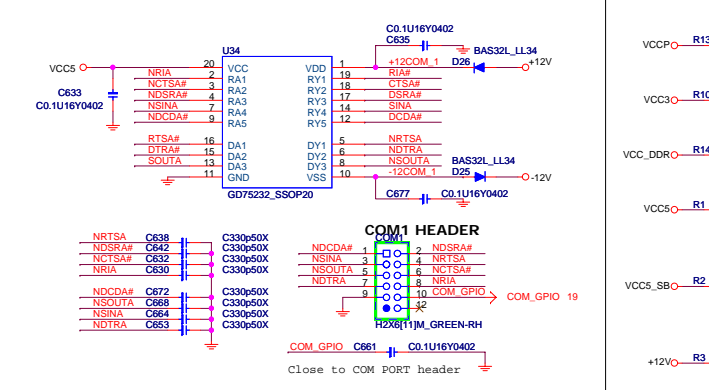
BIOS WRITE PROTECT



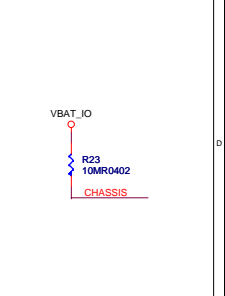
SERIAL PORT 2



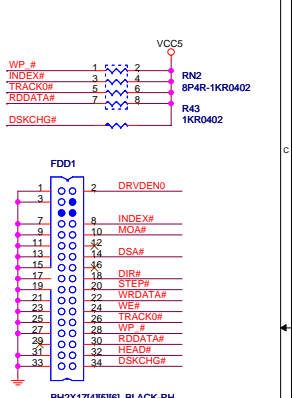
SERIAL PORT 1



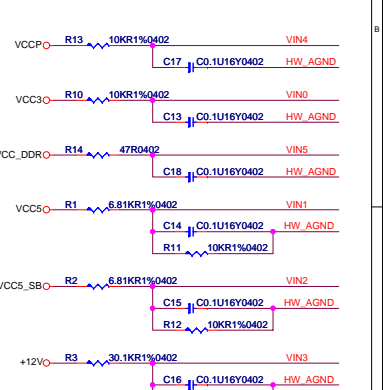
Super I/O Chassis



FLOPPY CONNECTOR

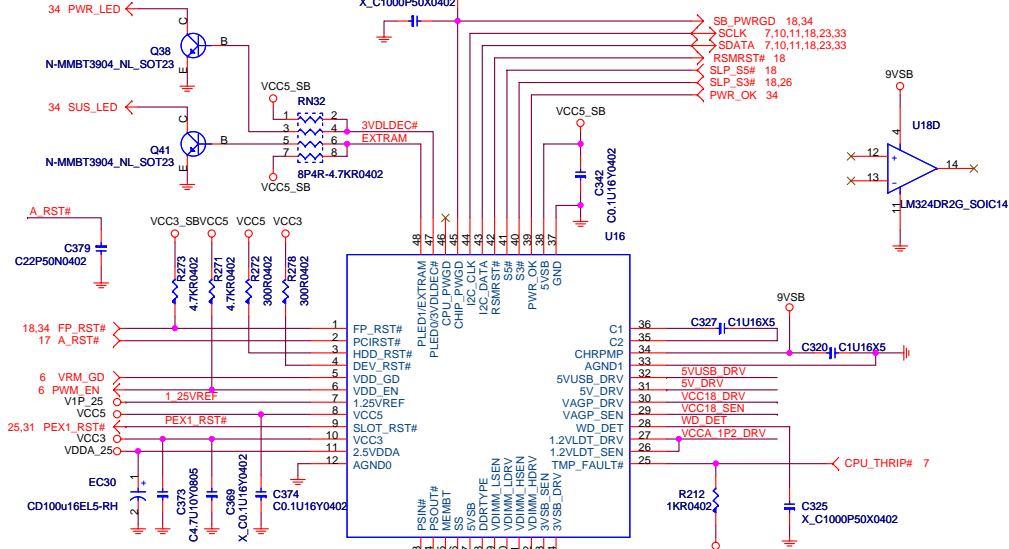
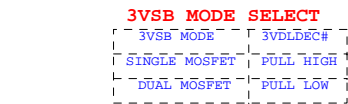


Thermal Resistor

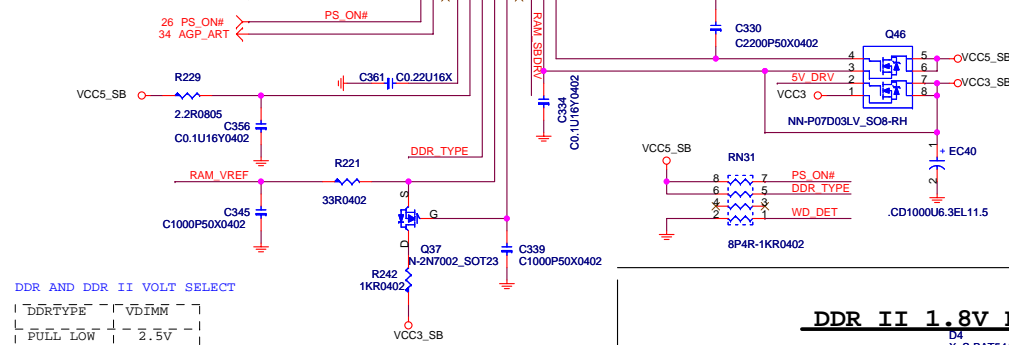


MSI
Link to the Future
MICRO-START INT'L CO.,LTD.
Title
LPC I/O IT8718F
Size
Custom
Document Number
L-A780
Date
Monday, September 17, 2007
Sheet
26
of
36
Rev
0C

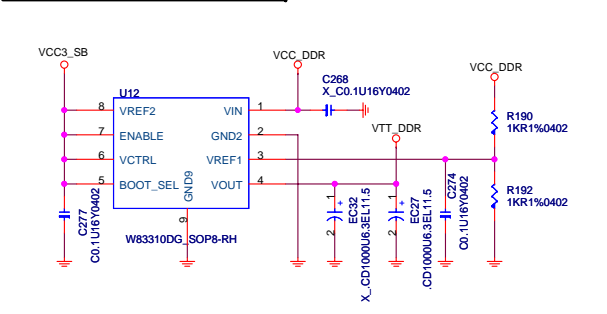
ACPI Controller



CPU VLDT Power

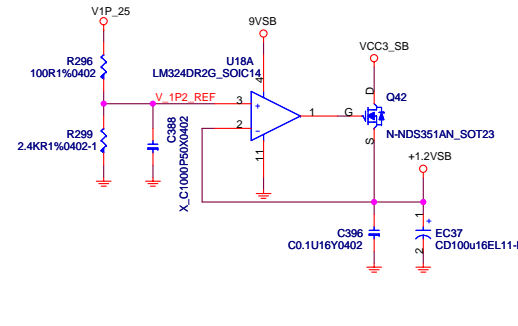


DDR II VTT POWER

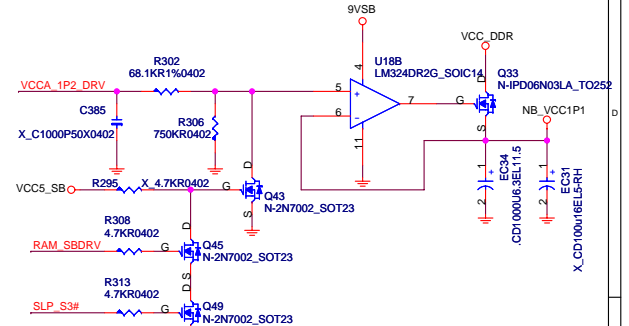


NB RS780/SB700 CORE POWER

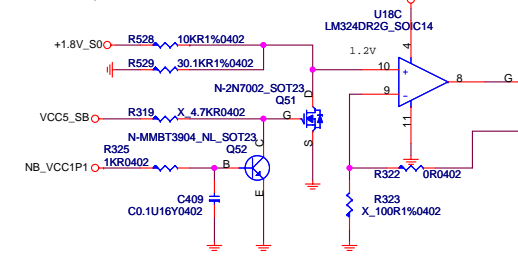
For SB +1.2V_SUS Power Rail



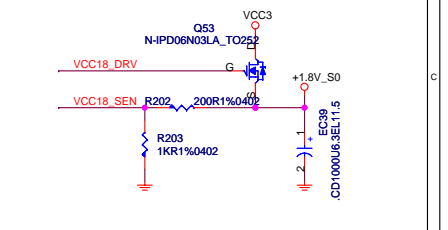
For NB +1.1V_SUS Power Rail



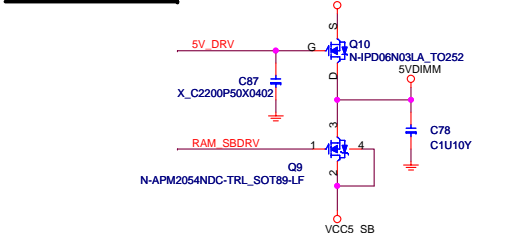
For CPU, NB & SB +1.2V Power Rail



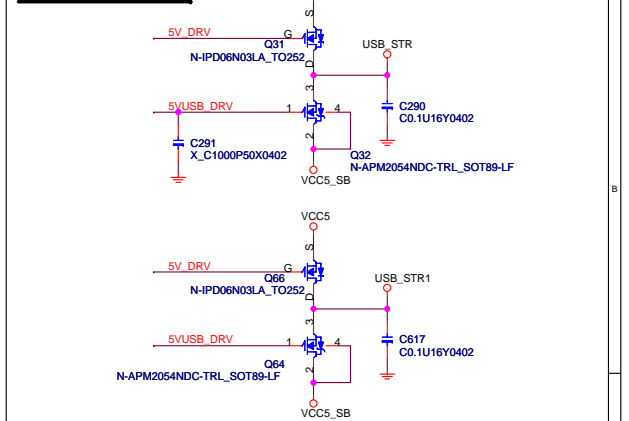
For NB +1.8V Power Rail



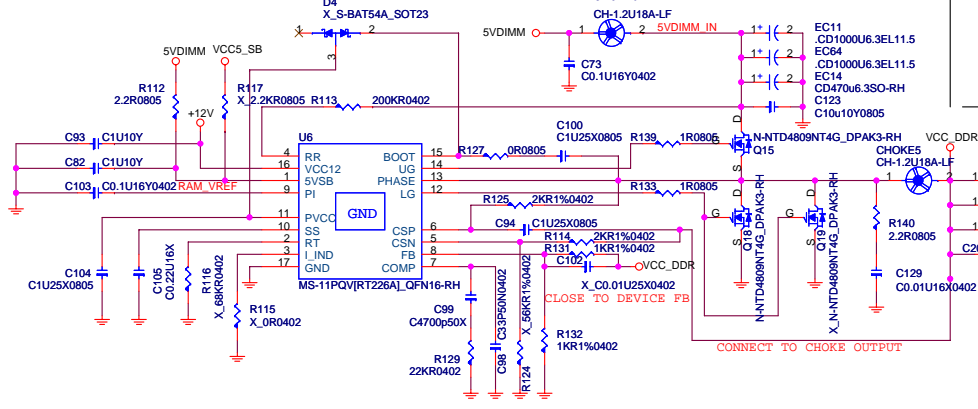
5V DIMM Power



5V DUAL Power



DDR II 1.8V POWER

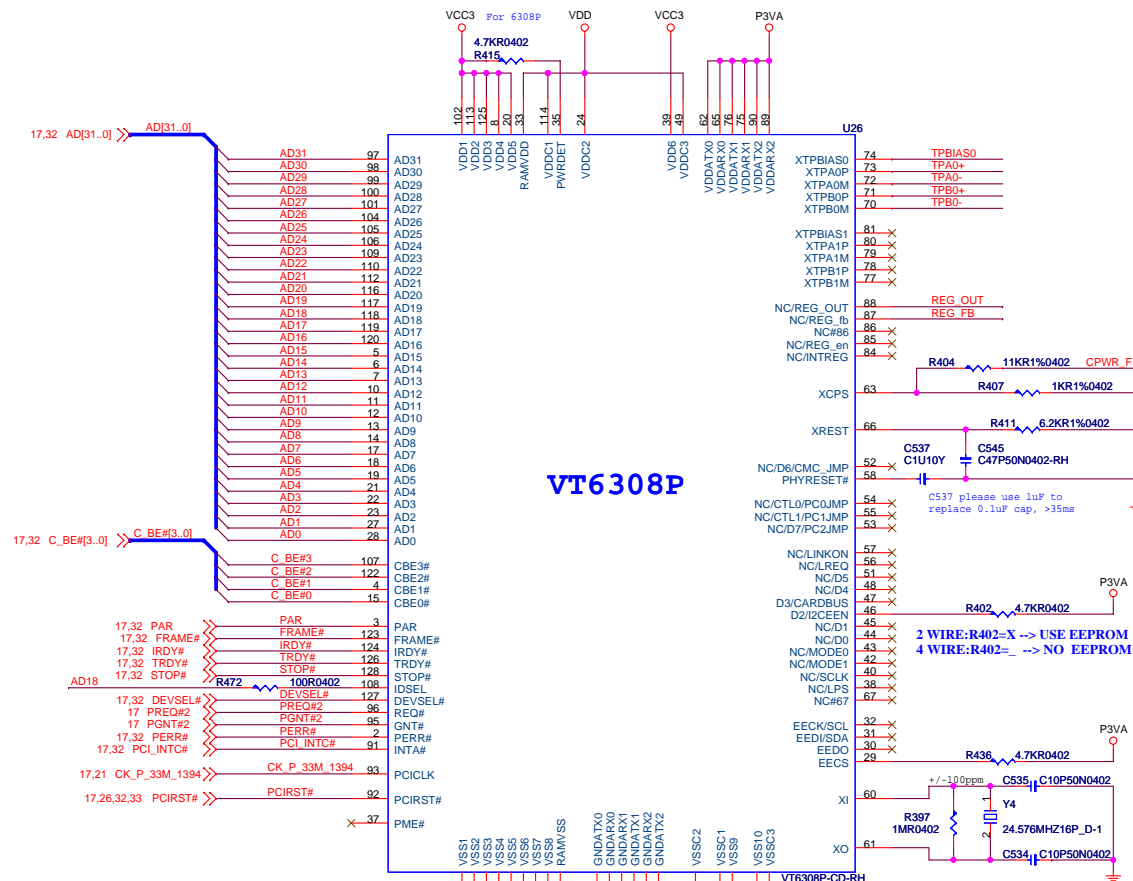


MSI
Link to the Future

MICRO-START INTL CO.,LTD.

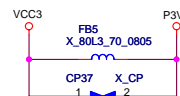
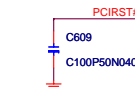
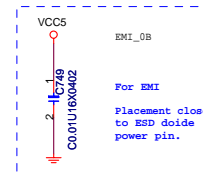
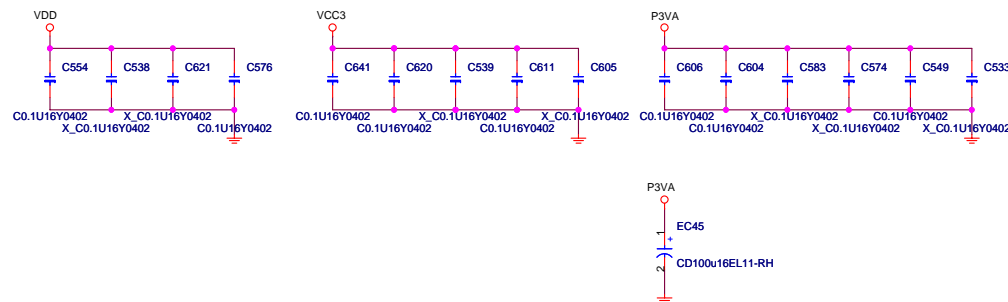
MS-6 ACPI Controller		Rev
Size	Document Number	OC
Custom	L-A780	
Date:	Monday, September 17, 2007	Sheet 27 of 36

IEEE-1394 VT6308P

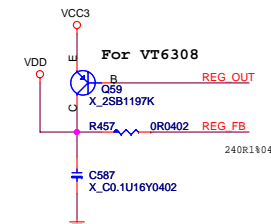
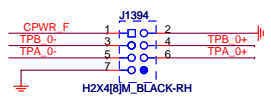
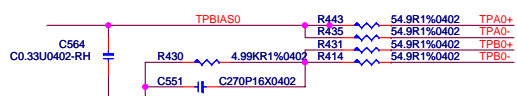
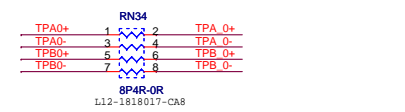
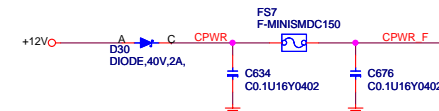
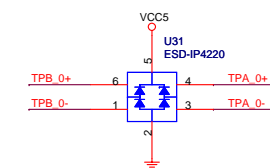


VT6308P

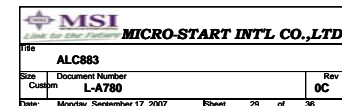
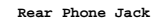
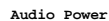
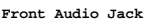
IDSEL = AD18
MASTER = PREQ#2
PCI_INT#
PCICLK#2



For IEEE-1394 ESD

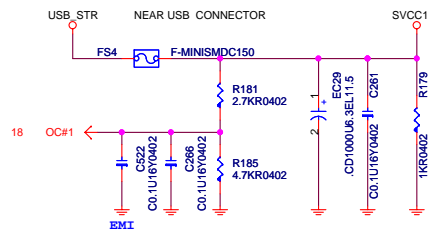


Default is ALC662



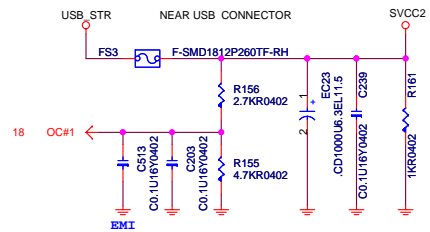
POWER CIRCUIT FOR USB PORT 0,1

Rear



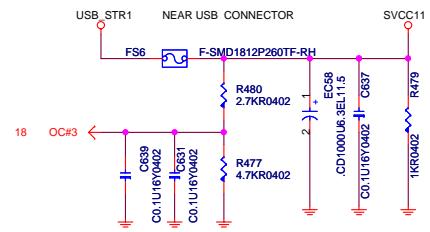
POWER CIRCUIT FOR USB PORT 2,3,4,5

Rear



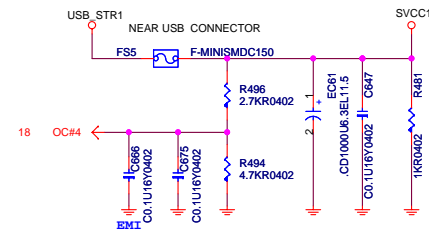
POWER CIRCUIT FOR USB PORT 6,7,8,9

Front

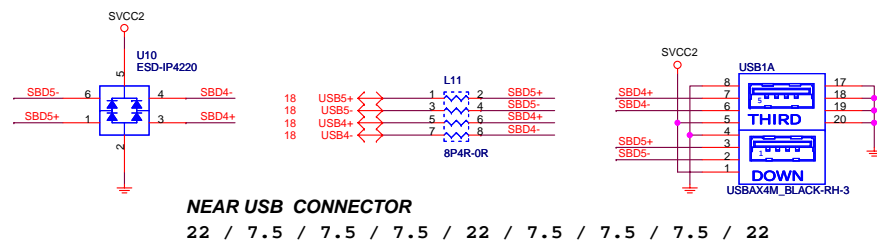
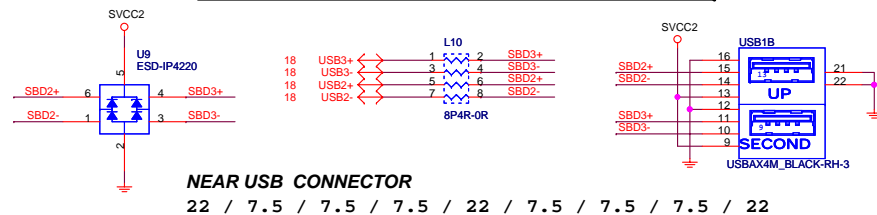


POWER CIRCUIT FOR USB PORT 10,11

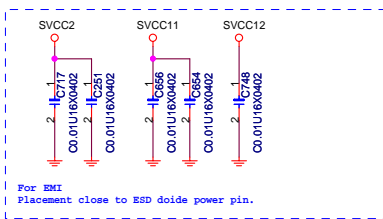
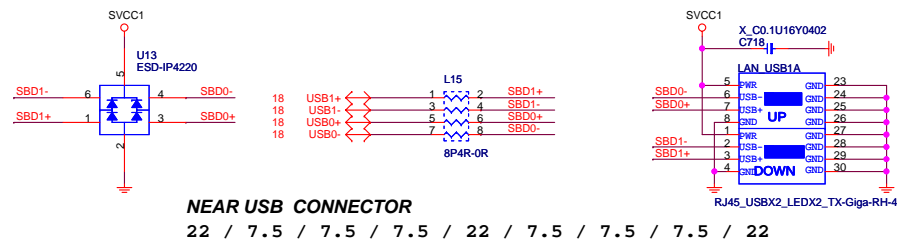
Front



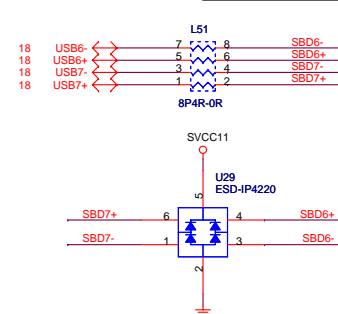
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



REAR PANEL USB CONNECTOR FOR USB PORT 2,3

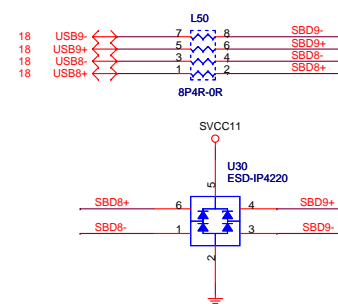


FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



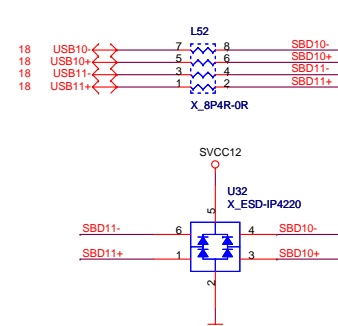
NEAR USB CONNECTOR
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

USB CARD READER + IR MODULE FOR USB PORT 8,9



NEAR USB CONNECTOR
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

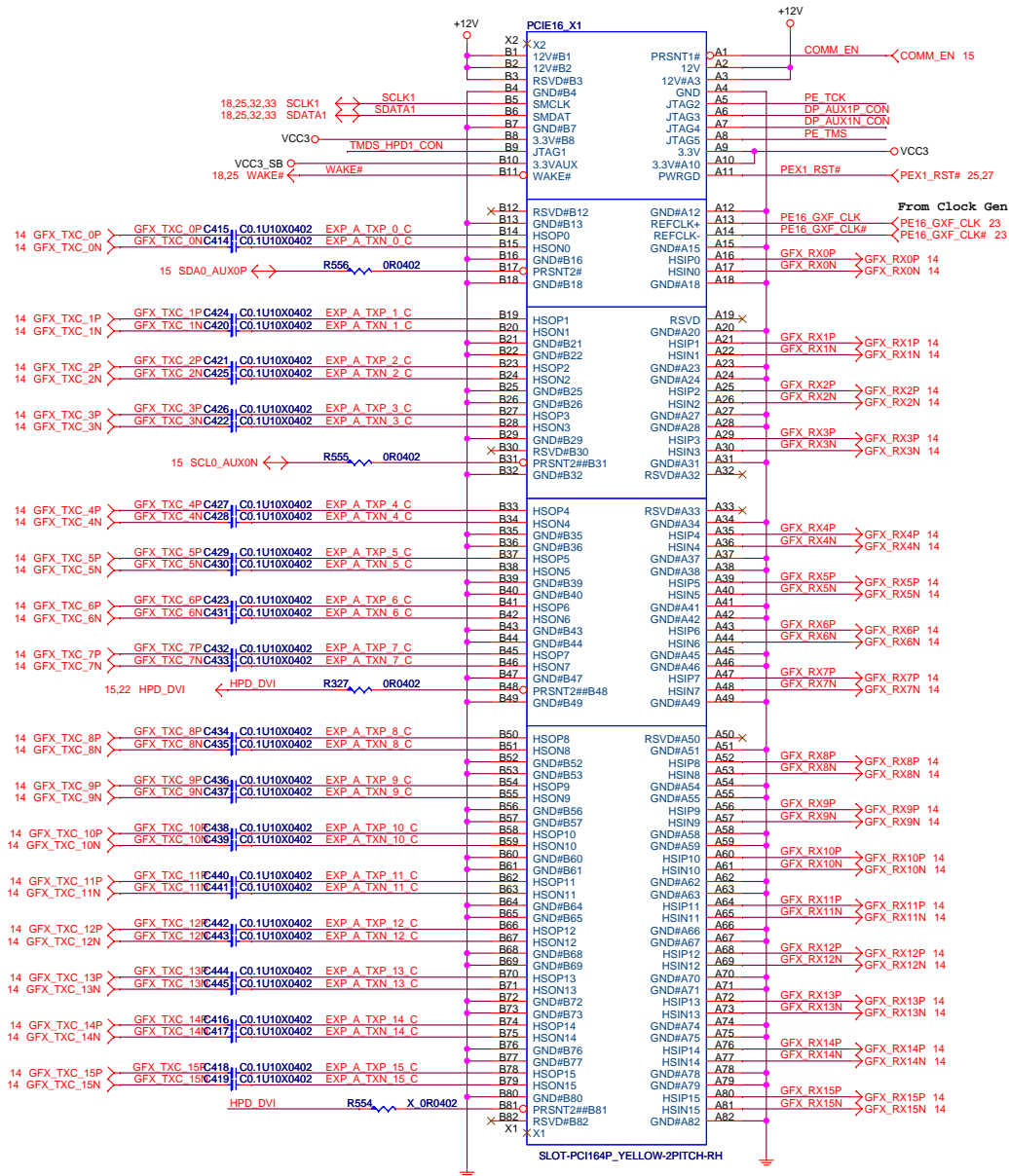
USB CARD READER + IR MODULE FOR USB PORT 10,11



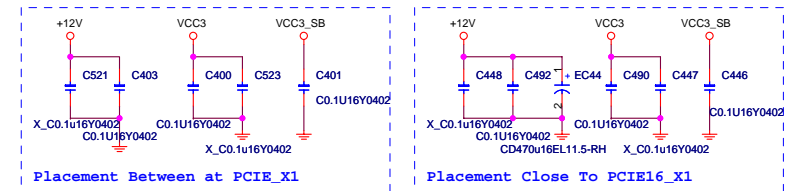
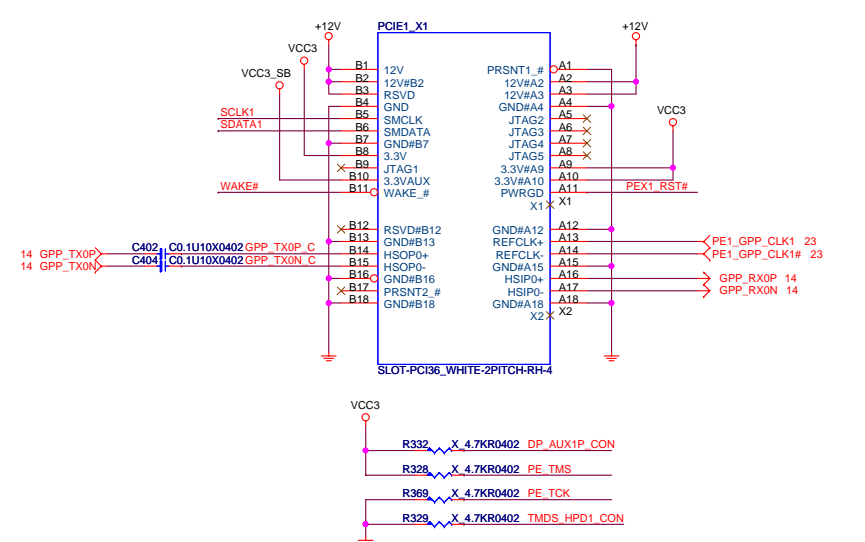
NEAR USB CONNECTOR
22 / 7.5 / 7.5 / 7.5 / 22 / 7.5 / 7.5 / 7.5 / 22

PCI Express Slot x16/x1

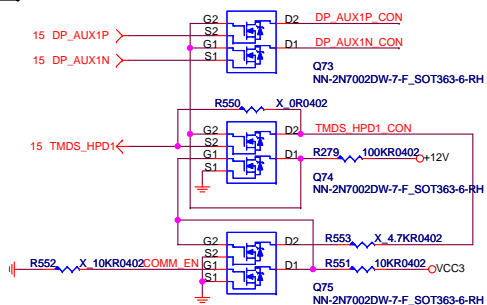
PCI EXPRESS x16 Slot

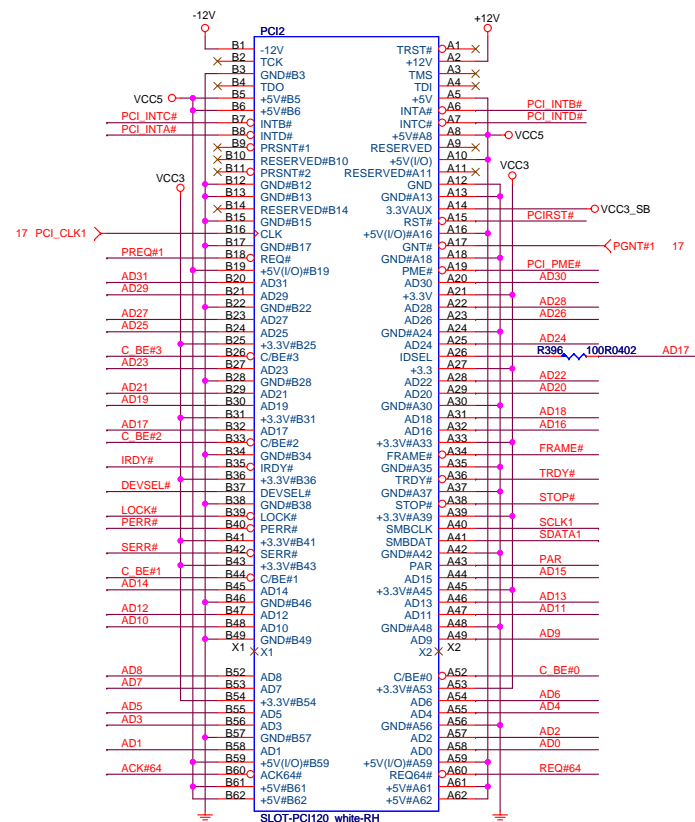


PCI EXPRESS 1 Slot-1



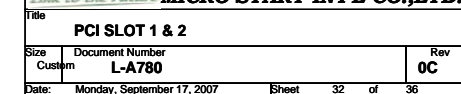
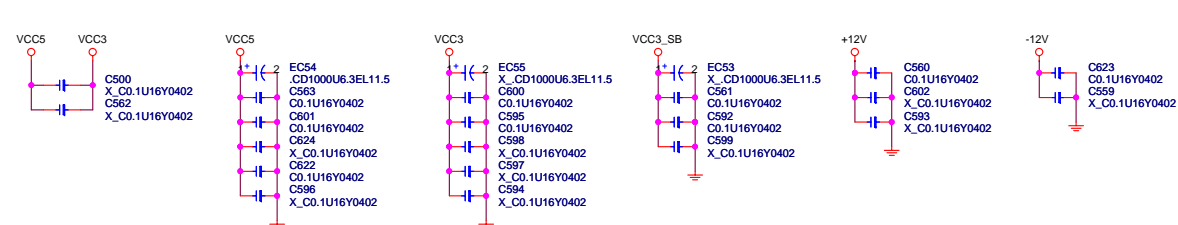
For Display Port



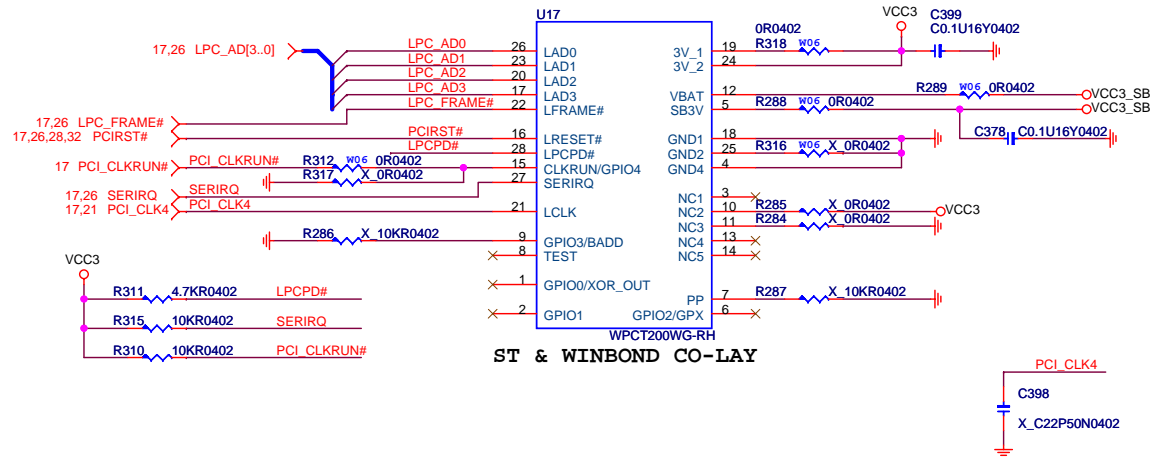
PCI SLOT 2 (PCI VER: 2.3 COMPLY)

```
IDSEL = AD17
MASTER = PREQ#1
PCI INT B, C, D, A
```

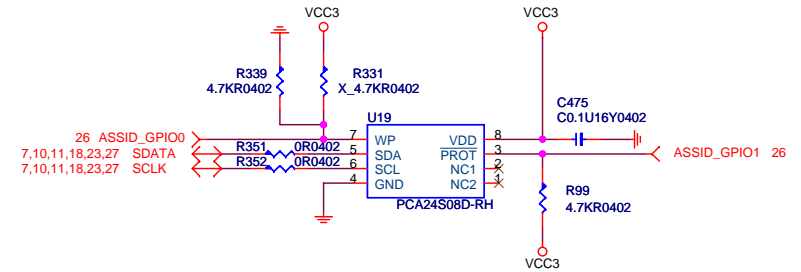
PCI SLOT DECOUPLING CAPACITORS



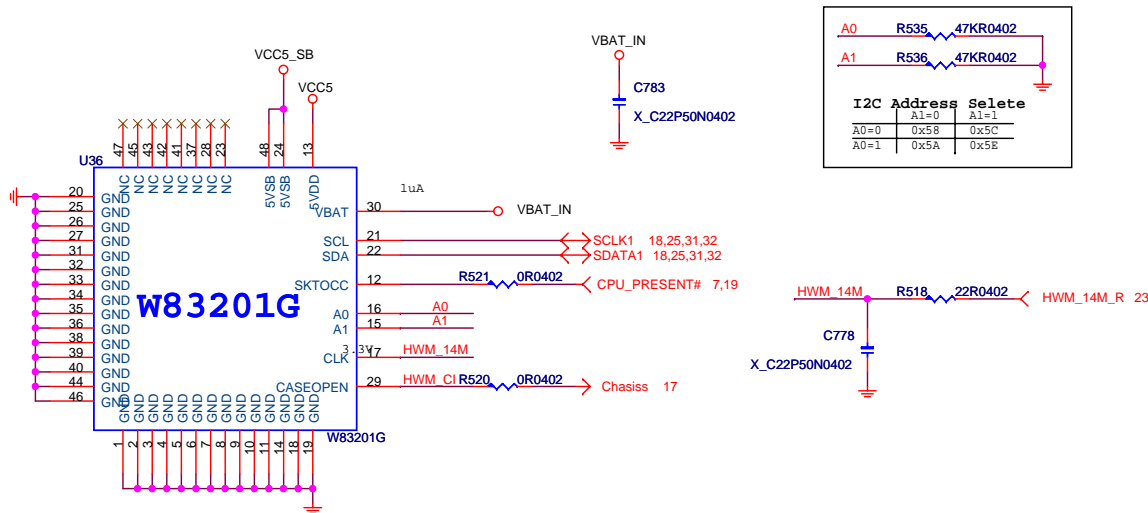
TPM Chipset



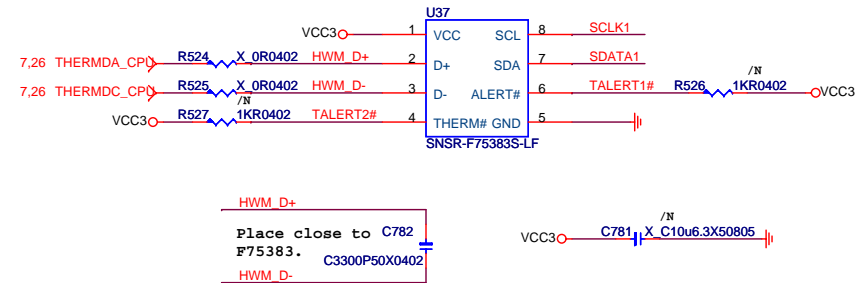
ASSET ID Chipset




ASF2.0 Hard Ware Monitor

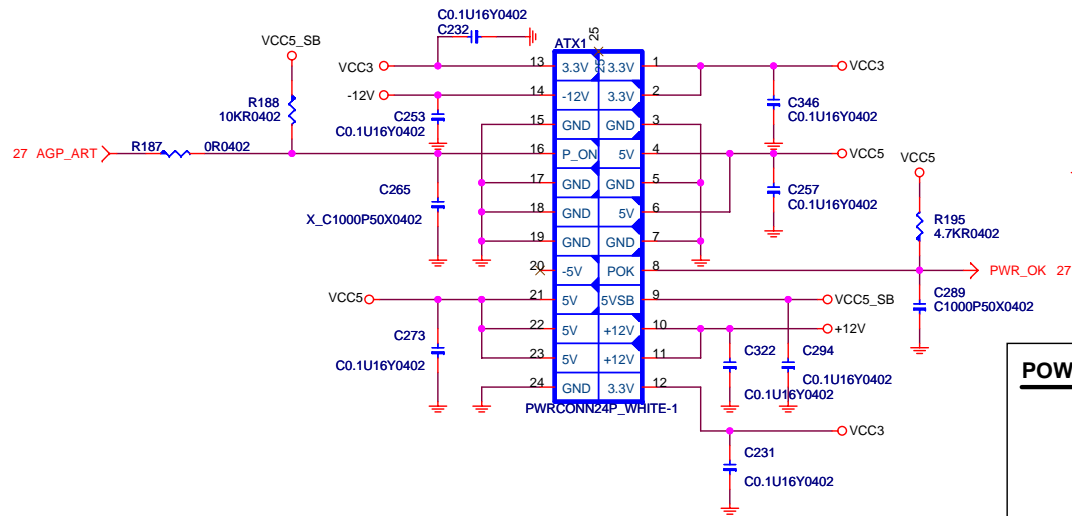


CPU Thermo Sense

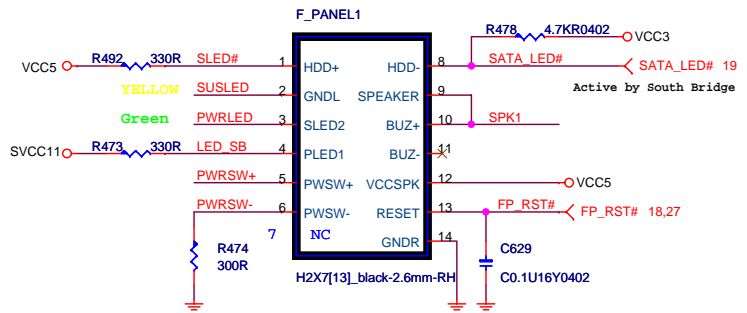


 MICRO-START INTL CO.,LTD.		
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TMP/Asset ID/HWM W83201G		
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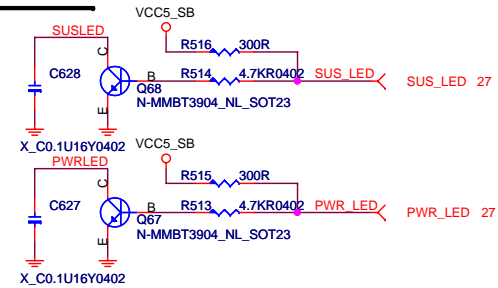
ATX CONNECTOR



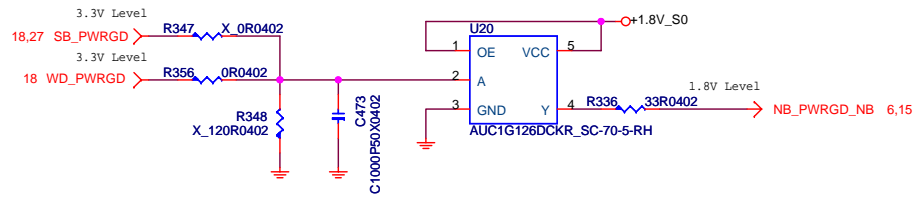
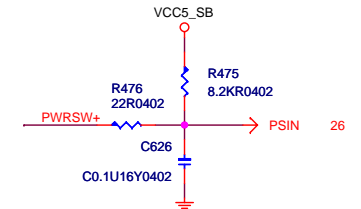
LENOVO Front Panel Connector



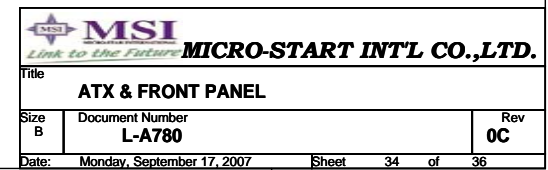
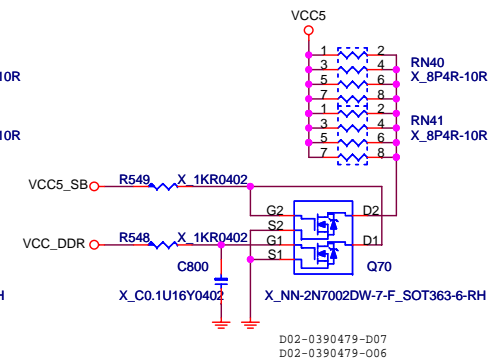
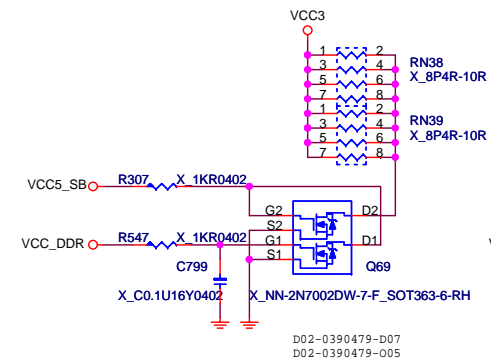
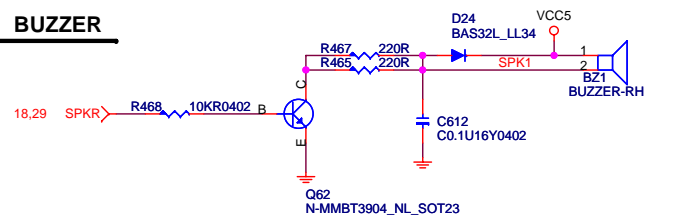
POWER LED



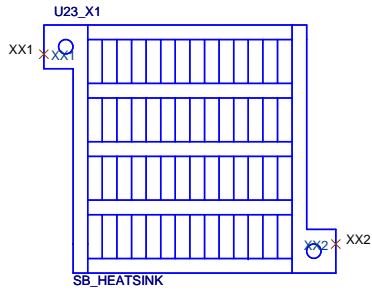
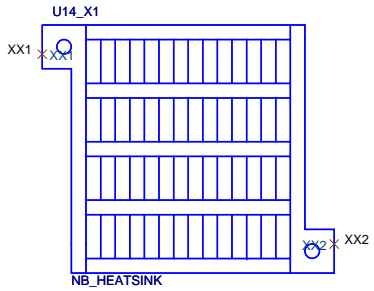
POWER BUTTON



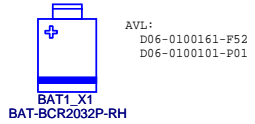
BUZZER



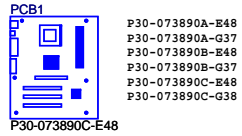
HEAT SINK



MANUAL PART

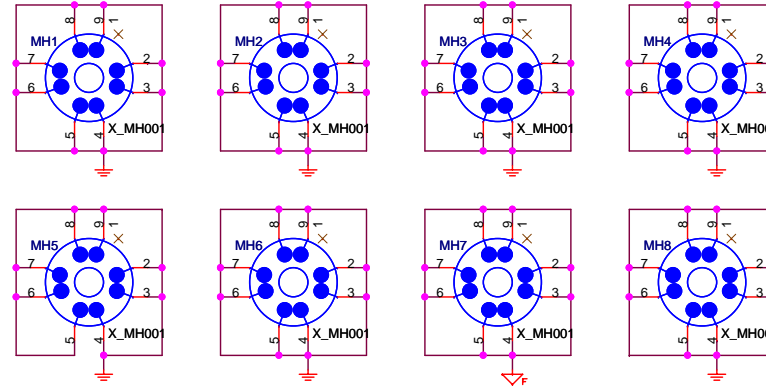
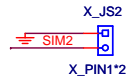
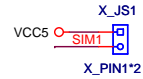


AVL:
D06-0100161-P52
D06-0100101-P01

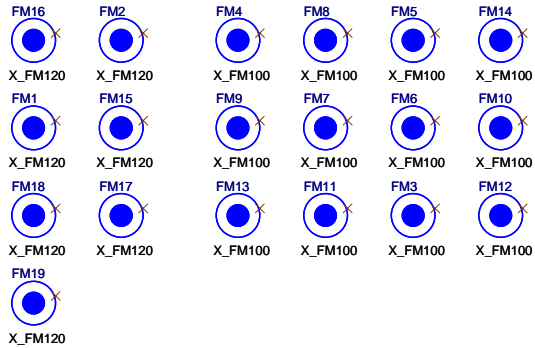



P30-073890A-B48
P30-073890A-G37
P30-073890B-B48
P30-073890B-G37
P30-073890C-B48
P30-073890C-G38

Simulation



Optics Orientation Holes



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History

Item	History	Date	Page
1	Version:0.1		
1	For RX780, stuff U20(T70-T4712620-T07).	07/01	34
2	For Power Good signal : R356 change to 330hm, add C473 with 1000pF, remove R340 and R341	07/01	34
3	For VDDA18HTPLL Power(RX780) : Stuff L28(L02-2218063-T19)	07/01	15
4	VCC_1V2 reference power source : single-handed reference power source with 2.4KR1% and 4.99KR1%, power use the +1.8V_50.(please see rework list)	07/01	27
5	For NB_VCC1P1 sequence : remove R295.	07/01	27
6	VRM Enable : Enable from MS-6 pin-6. Remove R38 · R36 · Q3 · C20. Short R48 and Q3 B-C.	07/01	6
7	R196 & R197 Change to 1.21KR1%.	07/01	13
8	For SPI strapping : R372 change to 1Kohm, TP15 pull high to VCC3_SB power through a 10Kohm	07/01	18,21
9	R45 change to 100Kohm1%.	07/01	6
10	AM2 CPU can't boot issue : R165 stuff 300R0402.	07/01	7
11	Remove U31.	07/01	28
12	VRM solution : R4=560R · R18=N/C · C8=N/C · R19=59KR · R45=120KR · R33=200R · R31=150R · EC19, 15=N/C · C713=N/C · Q14, Q20, Q23=D03-0480900-O05	07/25	6
13	DDR Power solution : C99=4.7nF, Q15, 18=D03-0480900-O05.	07/26	6
14	Solve LED issue:R513 ~ R516 · Q67 and Q68, add circuit.	08/03	34
15	Swap SBD11- & SBD11+ trace to solve circuit error issue.	08/03	30
16	Add W83201G circuit.	08/03	33
17	Add EC63 for VCC5_SB power.	08/06	27
18	Change IEEE-1394 ESD protection Diode Power from +12V to VCC5.	08/06	28
19	Add C779 and C780 for ESD reserve. Place close to Clock Gen side.	08/06	23
20	To modify NB_PWGRD to SB_PWGRD. This is creat net name issue.	08/06	34, 27
21	Add F_AUDIO_X1 Jump for Front Audio.	08/06	29
22	Add system vendor ID(SYS_ID0 & SYS_ID1) for customer.	08/06	26
23	C473 From 0.22uF/0603 cahnge to 1000pF/0402.	08/06	34
24	Change R408 from 10 K ohm to 3Kohm, and empty it.	08/06	17
25	change SB700 SB_PE PVDd power sequence control circuit from to 0R short.	08/06	17
26	change Q58 from 2N7002 to FAIRCHILD/ND5351AN (D03-351AN09-F01), empty it.	08/06	17
27	SPI strapping : R372 change to 1KR0402 and pull high R530 through a 10KR0402.	08/06	21
28	Add R531 to GND through 300ohm.	08/06	7
29	Change CHOKE5 from 1.1uH to 1.2uH.	08/06	27
30	change Q8 and Q13 level shift power to 5V, to solve layout issue.	08/13	22

Item	History	Date	Page
32	Remove R304 - R239 - R276 - R307, there are not need for RS780.	08/14	15
33	Change EC31 from 1000uF to 100uF to solve layout spacing issue.	08/14	27
34	Add Temperature sense header for customer require.	08/15	26
35	ADD R546 & R249 for MB_ID use.		
36	Update Realtek Audio reference circuit v0.3. AVDD5 power, 75ohm resistor, sense route and front panel. Version:0.2	08/21	29
37	Add R220 715ohm1%0402.	9/6	15
38	Remove R249.	9/6	15
39	Remove R213 & Q35, RS780 not need.	9/6	15
40	Remove L27 & L17.	9/6	15
41	Empty R230 and Stuff R232 for RS780 strap.	9/6	15
42	Stuff R291 for RS780 strap.	9/6	15
43	Empty R225 and Stuff R227 for RS780 strap.	9/6	15
44	Change Q40 & Q48 from 2N7002 to MMBT3904 for level shift RS780 issue.	9/6	15
45	Add R31 150ohm1%0402 for BOM error.	9/6	15
46	Change R530 and R372 to 2kohm for SPI ROM strap	9/6	21
47	Stuff R147 - R141 - R142 - R148 - R145 - R149 - D7 - D5 - D6 - D8 for RGB circuit BOM error.	9/6	22
48	Change and stuff R234 with 0R0402 Change and stuff R226 with 0R0402.	9/6	22
49	RQ change CPU FAN control from 3-PIN to 4-PIN : delete Q2 - R40 - R41. Add R29. Change CPU_FAN1 from 3-PIN to 4-PIN.	9/6	24
50	RQ change SYS FAN control from 3-PIN to 4-PIN : delete Q36 - R199 - R200. Add R228. Change SYS_FAN1 from 3-PIN to 4-PIN.	9/6	24
51	RQ change CPU FAN and SYS FAN control from 3-PIN to 4-PIN : Empty U2 - C46 - C47 - C45.	9/6	24
52	Add D34 circuit to support wake on ring function.	9/6	26
53	Add R98 - R86 - R523 - R87 - R546 - R239 to support custom system ID.	9/6	26
54	Empty R319 and R295 for sequence debug.	9/6	27
55	Change EC21 to Q3C for ME requirement.	9/6	27
56	change R528 to 10kohm1% and change R529 to 30.1Kohm1% for AMD RS780 A11 bug issue	9/6	27
57	Modify audio circuit to follow Realtek reference circuit. Add R558 & R557. Move D23 to +12V side and R901. Change Front Panel AC_HP_SNS circuit.	9/6	29
58	Reserve Q69 & Q70 minimum loading circuit.	9/6	34
59	change PCB to P30-073890B-E48	9/6	35

[illegible]